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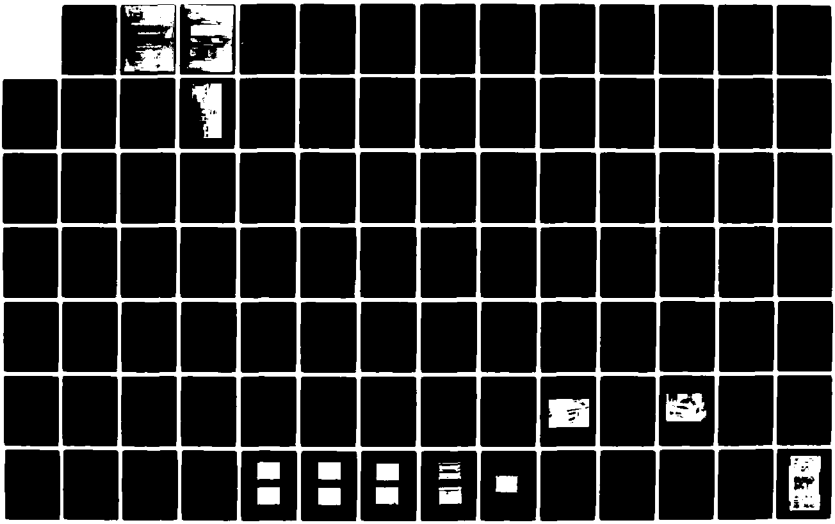

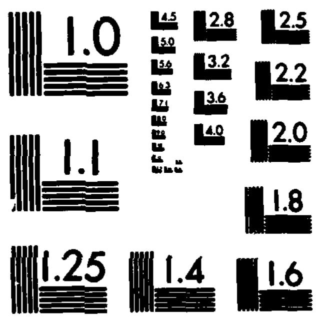

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Data compression	Optical scanning	Solid-state scanners
Image acquisition	Photodiodes	Video processing
Image processing	Run length coding	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the effort described herein is to provide technical consultation, equipment, and support services to the US Postal Service that will contribute to the development of the system definition of future electronic mail processing systems. Included in the scope of effort are investigations of high-speed image scanning technology, image frame memory storage, and image enhancement as well as fabrication of a scanner/frame-store memory test assembly. The seventh annual report briefly describes the individual efforts of the reporting period in an executive summary and provides in-depth data in five appendixes: Appendix A, Memory Technology Assessment; Appendix B, Image Acquisition Studies; Appendix C, DOD Facsimile Data Compression Standard with

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18. Previous annual reports:

First Annual Report, Advanced Mail Systems Scanner Technology, NOSC Technical Report NELC TR 1965, 22 October 1975, DTIC AD A020175

Second Annual Report, Advanced Mail Systems Scanner Technology, NOSC Technical Report NELC TR 2020, October 1976, volume 1 (Executive Summary and Appendixes A-F), DTIC AD A039962; volume 2 (Appendix G: Proprietary Supplement, High Speed Imaging Device); DTIC AD B018468L (now released for unlimited distribution)

Third Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 170, October 1977, DTIC AD A051508

Fourth Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 358, October 1978, DTIC AD A070546

Fifth Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 520, October 1979, DTIC AD A089436

Sixth Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 642, October 1980, DTIC AD A097493

Also see:
CCD Page Reader for Mail-Scanning Applications, Final Report for period 15 March 1976 to 15 May 1977, RCA Princeton Laboratories Report PRRL-77-CR-42, DTIC A062399

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Alexandria, VA 22314

20. Continued

Performance Comparisons; Appendix D, Preliminary System Architecture for a Modular Remote Video System (MRVS); and Appendix E, Hardware Illumination Correction and Hardware Edge Enhancement Performance Evaluation.

OBJECTIVES

1. Provide for the US Postal Service the consultation, equipment, and support services that will contribute to the generation and improvement of advanced mail transmission systems such as International Electronic Posting (INTELPOST) and Electronic Computer Originated Mail (E-COM). Include in this scope of effort: (1) investigations of scanner technology; memory technology for storage, sorting, and retrieval of messages and images; and data compression technology including error detection and correction (EDAC) and (2) the design, fabrication, and operating support of a scanner/frame store memory test assembly.

2. Contribute to the selection of the optimal devices, equipments, and techniques for high-speed image acquisition. Provide reliable designs of high-speed image processing logic that will preserve the quality of the image while reducing the image storage and transmission requirements and that will minimize the vulnerability of the image information to noise during processing, transmission, storage, sorting, retrieval, and reproduction.

3. Act as technical consultants to the USPS Office of Electronic Mail Systems Development in preparing technical requirements and statements of work and in evaluating technical proposals and contractor performance. Also, perform technical evaluation of contractor-produced developmental equipment.

RESULTS

1. The capability of the Image Capture and Analysis System (ICAS) has been greatly expanded during the reporting period.

2. Principal component additions to ICAS were the Hardware Illumination Corrector (HIC) and Hardware Edge Enhancer (HEE). These are two very high speed units which accept scanned image data at up to a 20 megapel per second rate and perform the functions of flattening the spatial illumination profile and improving the edge definition of acquired facsimile data.

3. The capability of ICAS to operate on digital image data was expanded from only 6 bits per pel to include 6-bit or 8-bit digital operations.

4. A new scanner characterization optical bench, Scanner III, has been fabricated and is in operation. The bench is instrumented to supply control clocks and bias-level voltages for the characterization of a wide variety of CCD imagers. Four parallel 8-bit 20-MHz analog-to-digital (A/D) converters are available to digitize the imager output channels.

5. The time-delay and integration (TDI) imager has been received from RCA Princeton Labs. All support electronics for the device have been fabricated and are incorporated into Scanner III. Characterization of the device has been started.

6. A contract has been let to Delta Information Systems for the study of image compression techniques. Tasks under this contract include compression analysis, effects of scanner noise, and effects of spatial filtering. The final project report is due in September 1982.

7. A memory technology study is in progress. The goals are to identify candidate memory systems, components, and techniques for the storage and sorting requirements of future electronic mail systems. Results to date are available in this report.

8. Progress has been made on the compressibility of image data both for transmission and for storage and retrieval. The technique of error detection and correction has been

included in the study. The use of 8-bit hardware illumination correction along with a simple form of selective filtering increases the image compressibility to a considerable extent.

FUTURE NOSC PLANS

IMAGE ACQUISITION STUDIES

1. Characterize the uniformity, accuracy, and stability of the analog circuits and 8-bit A/D converters presently incorporated into Scanner III.

2. Process a few color images using 8 bits per pel for comparison with previous 6-bit acquisitions.

3. Characterize the RCA time-delay and integration (TDI) imager for acquisition speed, sensitivity, noise, and cosmetic uniformity.

4. Evaluate the USPS R&D Labs laser scanner to assess suitability for high-speed, high-resolution scanning.

5. Study methods for semiautomatic generation of image origination, destination, and control information.

IMAGERY AND DATA COMPRESSION STUDIES

1. Define error rates and characteristics for potential USPS transmission and storage media systems.

2. Evaluate effectiveness of several compression algorithms on typed, handwritten, and continuous-tone image documents.

3. Evaluate the effects of selective filtering on compressibility.

4. Equate EDAC to transmission and storage media error rate and demonstrate error recovery capability.

5. Analyze size and resolution requirements for image logos and signatures. Study feasibility, complexity, and cost trade-offs of several methods of providing these features for future electronic mail systems.

MASS STORAGE STUDIES

1. Periodically review cost, reliability, and performance of state-of-the-art large buffer memory media and contribute to the formulation of USPS image and control memory technology requirements.

2. Identify candidate electronic mail system architectures where logo and/or subsequent images might be prestored at delivery destinations for subsequent merging and printing on a multiplicity of documents.

IMAGE PRESENTATION STUDIES

1. Analyze the requirements for the display of remotely scanned image data such as rejected optical character recognition (OCR) characters or non-machine-readable letter- and circular-class mail addresses. Include considerations for operator/machine interfaces to maximize throughput and accuracy and to minimize operator fatigue.

2. Study the parameters affecting human perception of image quality. Include factors of resolution, edge roughness, noise, contrast level, uniformity, and spatial distortion.

CONTENTS

CONTENTS

GLOSSARY

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A	Ampere
A/D	Analog-to-digital converter
A/R	Auto resolution
ASCII	American Standard Code for Information Interchange
B	Byte
b	Bit
BCH	Bose-Chaudhuri-Hocquenghem
BEP	Burst error processor
BER	Bit error rate
BILP	Beginning of intermediate line pair
BOLP	Beginning of line pair
bpi	Bits per inch
bps	Bits per second
CAS	Column address strobe
CCD	Charge-coupled device
CCITT	Consulting Committee on International Telephone and Telegraph
CED	Capacitance electronic disk
CMOS	Complementary metal-oxide semiconductor
CP/M ™	An operating system for microcomputers - trademark of Digital Research Corp.
CPU	Central processing unit
C/R	Compression ratio
CRAM	Calibration RAM
CV	Calibration value
DAV	Data available
DARCP	Display and refresh control processor
dc	Direct current
DEC	Digital Equipment Corporation
DIP	Dual in-line package
DM	Delay modulation
DMA	Direct memory access
DoD	Department of Defense
DRAM	Dynamic random access memory
DVM	Digital voltmeter
ECL	Emitter-coupled logic
E-COM™	Electronic Computer Originated Mail
EDAC	Error detection and correction
EDM	Engineering development model
E-NRZ	Enhanced nonreturn-to-zero
EOM	End of message
EOL	End of line

FAX	Facsimile
FBU	Frame buffer unit; format/buffer unit
FDS	First-difference statistics
FEC	Forward error correction
FET	Field-effect transistor
FRAM	Function RAM
FY	Fiscal year
FSM	Frame-store memory
GaAs	Gallium arsenide
GCR	Group-coded recording
GFE	Government-furnished equipment
GNAT	Company name for producer of microcomputers and their product line
GPIB	IEEE STD 488-1975 general-purpose interface bus for asynchronous data communications
HEE	Hardware edge enhancer
hex	Hexadecimal
HIC	Hardware illumination corrector
IBM	International Business Machines Corp.
IC	Integrated circuit
ICAS	Image Capture and Analysis System
IEEE	Institute of Electrical and Electronics Engineers
INTELPOST ™	International Electronic Post
ips	Inches per second
JPL	Jet Propulsion Laboratory
k	Kilo-; 1000 or 1024 depending on context
kbps	Kilobits per second
LDTB	Large drum test bed
LED	Light-emitting diode
lp/mm	Line pairs per millimeter
LSB	Least significant bit
LSI	Large-scale integration
LSM	Letter sorting machine
M	Mega-; million or 2^{20} depending on context
MBA	Mass bus adapter
MCU	Memory control unit
MIU	Memory interface unit
mm	Millimeter
MOS FET	Metal-oxide semiconductor field-effect transistor
MRVS	Modular remote video system
ms	Millisecond
MSB	Most significant bit

MTBF	Mean time between failures
MUX	Multiplexer
mV	Millivolt
mW	Milliwatt
NATO	North Atlantic Treaty Organization
NEC	Nippon Electric Corporation
n-MOS	N-channel metal-oxide semiconductor
NOSC	Naval Ocean Systems Center
OCR	Optical character recognition
PBS	Pel brightness statistics
PC	Personality chassis
pc	Printed circuit
pel	Picture element
P_{in}	Input pel
PN	Pseudorandom number
P_{out}	Output pel
PPHE	Printer and paper-handling equipment
PROM	Programmable read-only memory
RAM	Random-access (read/write) memory
RAS	Row address strobe
RCA	Radio Corporation of America
R&D	Research and development
R, G, B	Red, green, and blue
rpm	Revolutions per minute
RTC	Return to control
SBI	Synchronous backplane interconnect
SCF	Sectional center facility
SDTB	Small drum test bed
SFI	Spatial frequency identification
SOM	Start of message
SPO	Serving post office
TDF	Tactical digital facsimile
TDI	Time-delay and integration
TDMA	Time-division multiple access
T/H	Track and hold
tpi	Tracks per inch
TTL	Transistor-transistor logic
μ	Micro (millionth)
USPS	United States Postal Service
VAX	Virtual address extension

VHD	Video high-density optical disk
vhf	Very high frequency
XOR	Exclusive OR

EXECUTIVE SUMMARY

EXECUTIVE SUMMARY

PROGRAM GOALS

The major goals of the Scanner Technology Program thus far have been to identify and resolve problems associated with producing digital equivalent images from a wide variety of hard-copy documents at very high speed. The future-plans overview, presented earlier in this summary, gives some indication that the primary emphasis of image acquisition is being softened as solutions to USPS image acquisition problems have been found. The Image Capture and Analysis System (ICAS) can now demonstrate most of the current USPS image acquisition goals. Goals from the FY81 Statement of Work follow:

- High Quality Image Acquisition
  - Either orientation of 8-1/2- by 11-inch documents
  - Typed, handwritten, or continuous-tone images
  - Monochrome or color images
  - Resolution up to 200 by 200 or 300 by 300 pels per inch
  - Up to 84 megapels (504 megabits) per second
  - Image Enhancement
    - Edge enhancement
    - Nonlinear video techniques
    - Thresholding
    - Color filtering
- Image Bandwidth Compression Techniques
  - Run-length encoding
  - Walsh, slant, or Fourier encoding
  - Block void encoding
- Mass Memory Studies
  - Imagery memory technology
  - Memory buffers for imagery applications
  - Image storage, sorting, and retrieval
  - Error detection and correction

1981/1982 TASKS

This report is the seventh in a series of annual summary reports and covers the period 1 October 1980 to 30 April 1982. During this reporting period, tasks were reasonably well balanced among the four categories of hardware, software, support, and documentation deliverables. The categories and the tasks within each are described in the following paragraphs. (Data on previous annual reports are contained in block 18 of the enclosed Report Documentation Page, DD1473.)

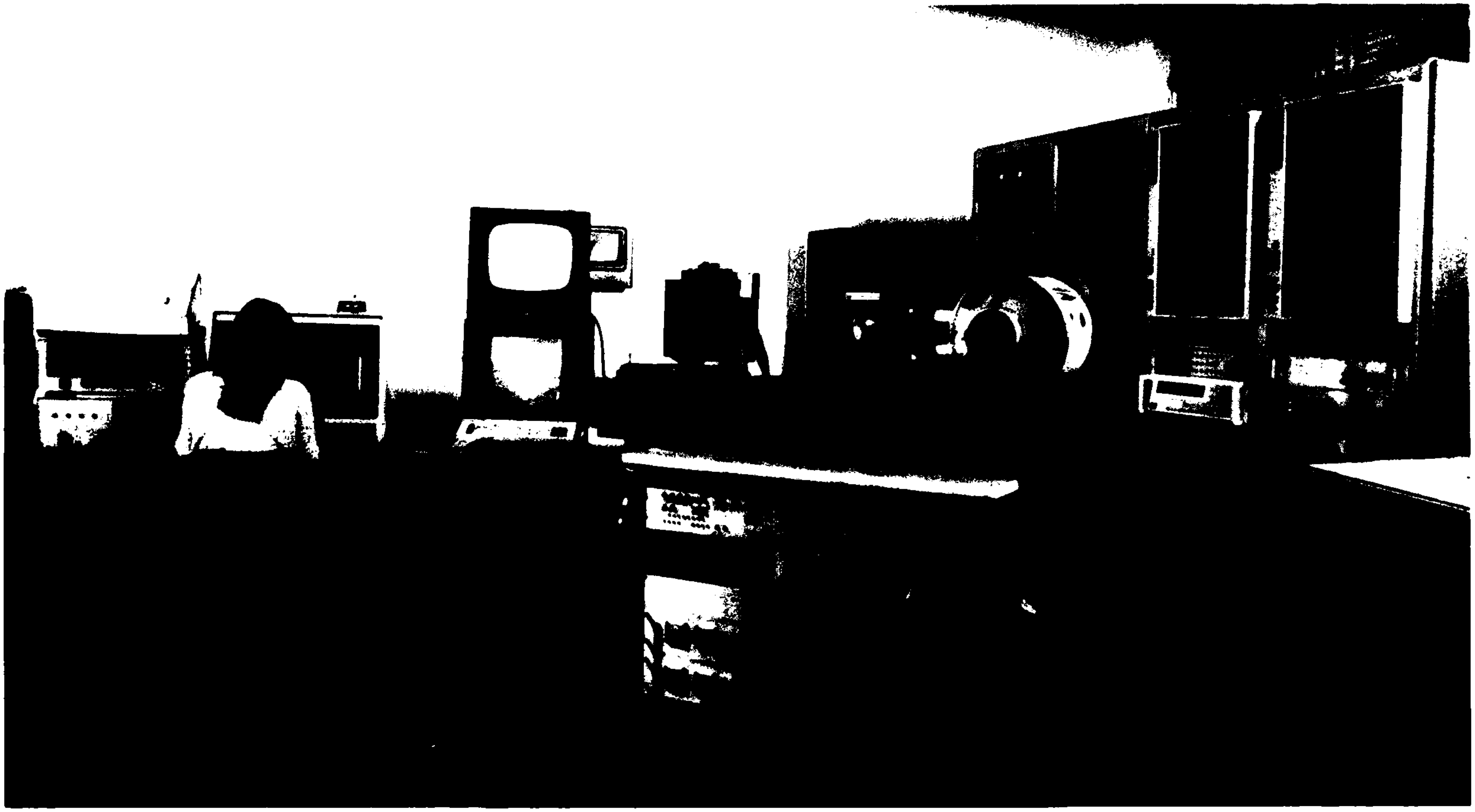

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Figure 1. ICAS with RCA TDI imager instrumentation on Scanner III.

HARDWARE ACCOMPLISHMENTS

Scanner III

Scanner III is a third-generation optical bench designed for USPS image acquisition studies at NOSC. Started in FY80, the completed test apparatus provides a large drum for presentation of moving images, an illumination source, and accommodations for a variety of lenses, sensors, and support electronics. In the early part of the reporting period, full electronic support circuits were developed for acquisitions with the Fairchild charge-coupled device (CCD) Model CCD 143 line imager. Presently, Scanner III is fully instrumented to characterize the RCA time-delay and integration (TDI) CCD Model TC 1262 imager. A detailed description of Scanner III is contained in appendix B. Figure 1 is a photograph of the ICAS with the RCA TDI instrumentation mounted on Scanner III.

Hardware Illumination Corrector

Illumination correction is a process whereby the imager/lens is exposed to a white standard target that is illuminated by the standard system illumination source. The resulting response curve of pels across the scanned line (eg, 1700 or 2200 pels) contains information regarding the droop in illumination intensity at the edge of documents, the optical "cosine fourth" lens response losses, and any response anomalies of the individual photosites in the imager. By using a normalized reciprocal of this function curve multiplied pel by pel with acquired scan line image data, first order errors are removed from incoming digitized image data.

The ICAS used captured storedimages and a software routine to multiply a reciprocal white standard value (from a function table) by the received brightness value for each pel position along a scan line. The process was repeated for each scanned line (1700 pels per line X 2200 li = 3.74×10^6 pels per document), a laborious 20-minute process for ICAS software.

In FY81, a contract was let to Data/Ware Development, Inc. to design and fabricate a hardware illumination corrector (HIC) that can perform this process with either 6-bit or 8-bit pel data at up to 20 megapels per second. After the calibration random access memory (CRAM) is loaded, the HIC is placed in series with the incoming digitized video. The HIC output consists of digitized, illumination-corrected data. Acceptance tests were completed during the reporting period; subsequently the equipment has been performing well.

Hardware Edge Enhancer

Methods for providing edge enhancement have been studied by NOSC for several years. Software routines have been written to perform 3 by 3 kernel operations on bilevel and continuous-tone images by using a modified Sobel operator technique. Results from software-converted images showed definite improvement in the edge definition of typed and handwritten images with higher values of the algorithm gain constant.

Since the procedure requires intensive processing on each of the 3.74 million pels in a single-page image scanned at 200 by 200 pels per inch, real-time throughput using microprocessors and software routines is not possible. A contract for a special hardware edge enhancer (HEE) was let to Data/Ware Development, Inc. Using a 21-stage pipeline process, the contractor succeeded in delivering the HEE, which can operate with 6-bit or 8-bit pels at a throughput rate of 20 megapels per second. This unit is now interfaced to ICAS in the

serial digital data path after the HIC and before the ICAS personality chassis. The unit can be switched in or out of the data path, or it can be left in the path and given a processing gain constant of zero, all under the control of the ICAS Tektronix 4054 or of the GNAT 10 microcomputer furnished by Data/Ware under contract, to control the HIC and the HEE. The 21-stage pipeline delay is accounted for in the ICAS timing and control logic.

Personality Card Sets

The function of the personality chassis (PC) in ICAS is to convert any arbitrary input data format into 48-bit words in a standardized format acceptable to the memory interface unit (MIU) and the frame story memory (FSM). During early work, a simplified version of a personality card accepted 6-bit serial pels, arranged eight of them in sequence in a 48-bit buffer, and transmitted them to the MIU. When development work began (FY77) on the RCA time-delay and integration (TDI) charge-coupled device (CCD), another personality card set was designed to accept four 6-bit pels in parallel and to arrange successive groups of them into 48-bit words for transmission to the MIU. This card set accepts data simultaneously from each end of the scan line, ie two pels from the beginning of the line and two pels from the end of the line. This was to be the worst-case design that had to be accommodated by the PC. This card set was also used later, during the characterization of the Fairchild scanner designed for the printer and paper-handling equipment (PPHE). By the use of exchangeable plug-in cards, almost any input format can be converted to the fixed-format output acceptable to the MIU.

Two additional personality modules were developed during the reporting period. A single-card module was required to accommodate a single channel of either 6-bit (8 each per MIU word) or 8-bit (6 each per MIU word) image data from Scanner III for storage in the FSM. Operation is switch-selectable (6-bit or 8-bit) on the card. This module is compatible with the new 6-bit/8-bit software and allows characterization of the new Fairchild CCD 143.

A second module, a four-card set that has been designed and fabricated but not yet debugged, accepts the four adjacent pel output channels from the four separate ports of the RCA TDI imager and packs them into sequential 48-bit ICAS words. This card set also accepts either 6-bit or 8-bit data. For the preliminary checkout, this module is not needed. The four TRW A/D outputs are being multiplexed in Scanner III into a single serial stream of 8-bit pels. When the TDI chip is evaluated at the full output rate of 21 megapels per second per port, the second set of new PC cards will be debugged.

Comtal Image Processing System

A Comtal Vision One image processor is a subsystem of the ICAS hardware facility. It provides random access memory (RAM) storage for a continuous-tone 512- by 512-pel color image with 8 bits (256 levels) of intensity resolution for each of red, green, and blue (R, G, B), for color monitor display refresh. This Comtal unit has had several problems that were never resolved during acceptance tests and that have persisted for several years despite occasional attempts by NOSC technicians to diagnose the causes of the intermittent operational modes. During this reporting period, one of the more severe malfunctions was isolated and corrected by replacing a marginal integrated circuit. As technician time becomes available, the remaining problems of pattern-sensitive refresh memory storage and nonoperation of some of the display presentation commands will be investigated.

Lens Mount Design

The USPS has acquired custom-designed lenses for imaging work, from Alpha Optical, Inc. These lenses have an aperture of f/1.4 and a focal length of 92.8 mm. One of the lenses has been shipped to NOSC for use in our scanner studies. A new mount for the lens assembly, compatible with Scanner III, has been designed and fabricated.

SOFTWARE ACCOMPLISHMENTS

The software effort during the current contract year was divided between the development of new software and the upgrading of existing software to accommodate new hardware configurations.

Wire List

With the development of substantial new hardware, the task of generating and maintaining wiring documentation became cumbersome. A wire list software package was therefore developed to simplify the operations. (This effort was started at the end of the previous period.) The significant features of this package include variable card configuration, automatic multiple sorting modes ("to," "from," "module," and "signal name"), parts list maintenance, error checking, and simple operator interaction with immediate feedback.

At least six new circuit cards were designed with the aid of this package. Because of its simplicity of use and its versatility, an estimated 10% of the potential hardware development time was eliminated.

HIC/HEE

Substantial software development effort was made in conjunction with the correction and enhancement hardware. The effort was expended mostly in developing software test routines to assist the Data/Ware (contractor) engineers in the hardware debugging effort. The balance of the effort produced the operating routines such as table generation and transfer.

Scanner III Control

With the introduction of Scanner III into ICAS, automatic computer control of a number of scanning parameters was made available. These parameters include lines scanned, lines delayed, pels scanned, pels delayed, pel precision (6-bit or 8-bit), and resolution. In support of this capability, software was written to allow simple modification of the parameters either under program control or via the operator's console.

TDI Imager Control

In conjunction with the Scanner III development, a special set of software controls was provided to interface with the TDI imager currently being evaluated in ICAS. Special-purpose functions are provided to allow manipulation and transfer of the clock waveforms contained in the RAM card.

A/D Converter Testing

With the addition of on-line scanner control, the A/D converter test software has been upgraded to increase the sample rate and therefore the reliability of the test. Rather than acquiring data via the frame store memory, pels can be sampled directly from the scanner by a single 4054 read operation. This removes the MCU from the test loop and results in a much higher sample rate.

6-Bit/8-Bit Processing

The most significant software effort resulted from the fact that Scanner III is capable of acquiring images at eight bits of resolution, necessitating the generation of software that can perform 8-bit image processing algorithms. Because of memory capacity and soft-copy display capability, it was also necessary to retain the capability to process 6-bit images. Rather than retaining two separate sets of software, since pel access is different for different precisions, a scheme was devised to use the same software for either precision. This change required modification or rewriting of all existing image processing software, but it simplifies the development of new algorithms.

The key to the new approach is the maintenance of a set of image status and configuration parameters and the development of a set of "universal" subroutines. The parameters of concern include number of lines, number of pels per line, and number of bits of precision in the image as well as statistics buffer status. The subroutines include pel access routines that perform the access on the basis of the current parameter values, thereby making the current configuration irrelevant to an application (processing) program. This greatly simplifies the development of applications by relieving them of the bookkeeping burden normally associated with the varying configurations. The new program (ZOOM, for example) took only 2 hours to design, code, enter, and debug. Without the subroutines, this process would have taken between 6 and 8 hours.

A number of the current programs that will operate on either 6-bit or 8-bit images are upgrades of previously developed programs. The others consist of new programs that provide much greater flexibility and functionality than was previously available. The programs are summarized in tables 1 and 2.

All functions in table 1 have been upgraded to handle both 6-bit and 8-bit images as well as other improvements noted. The functions in table 2 are new and include the 6-bit/8-bit capability.

RESOLUTION	Improves and simplifies operation of resolution testing
STANDARD	Improves and simplifies operation of white standard acquisition
CURSOR	Manipulates a cursor on the high-resolution display (nondestructive)
ANNOTATE	Annotates images in memory. Now provides variable background and character brightnesses as well as interline and intercharacter spacing.
VERSATEC	Simplifies and speeds printing of images on Versatec printer/plotter

Table 1. Upgraded image processing programs. (Continued beyond this page.)

DICOMED	Simplifies and increases versatility of image printing on film, on DICOMED film recorder
FNTABLE	Now generates tables of up to 256 values
MINIFY	Simplifies and speeds minification of images
ANALYSIS	Simplifies and speeds analysis of images (PBS, FDS, SFI)
SAVSTATS	Saves statistics on tape
TXIMAGE	Transfers a portion of an image to the 4054
TRANSTATS	Transfers statistics to the 4054 (PBS, FDS, SFI)

Table 1 (Continued)

FILL	Places a constant in any rectangular portion of refresh memory
ALIOPS	Performs arithmetic and logical functions on two images: ADD, SUBTRACT, MULTIPLY, DIVIDE, AND, OR, XOR
FNMAP	Performs a function table mapping on an image
FILTER	Performs filter operations on an image
COPY	Copies part or all of image from memory or tape to memory or tape, in any of three formats
ZOOM	Magnifies an image by any integer factor to 64

Table 2. New image processing programs.

TECHNICAL SUPPORT

JPL Images For Compression

Specially formatted images were required by the Jet Propulsion Laboratory (JPL), Pasadena CA, under contract from the USPS, to perform compression studies. NOSC was requested to provide a number of computer tapes containing digitized images at resolutions of 200 by 200 and 300 by 300 pels per inch. These images were scanned in both the horizontal and vertical directions. They were furnished as both continuous-tone and bi-level (thresholded) versions. Copies of the tapes of these images, made from some 20 masters furnished by JPL, are in the NOSC/ICAS tape library.

Plain-Paper Printer Sample Measurements

The USPS obtained film strip test sample recordings of high-resolution deflected laser signals from Litton Datalog Corporation, Long Island, under USPS contract to design a high-performance, high-speed plain-paper printer. Some of these samples were sent to NOSC for evaluation of the uniformity of spatial position, beam diameter, and recorded optical density on the recording media. Results of these investigations were submitted to the USPS.

Delta Information Systems Contract

A contract was let by NOSC to Delta Information Systems, Inc. for the purpose of broadening the scope of effort in compressibility. The work is divided into three major tasks: Task 1, compression analysis, consisting of a first subtask of measuring compression ratios and a second subtask of investigating advanced compression techniques, including bilevel graphics and the coding of continuous-tone imagery; Task 2, measurement of the effect of scanner noise on compression; and Task 3, measurement of the effect of spatial filtering on compression.

Modular Remote Video System

NOSC was requested to develop a preliminary system architecture for a modular remote video system (MRVS). The purpose of this study was to initiate design of efficient off-line work stations for a multiplicity of key-entry operators, allowing them to accurately accomplish the mail sorting process on non-machine-readable letter- and circular-class mail at a high throughput rate. The results of this study are included as appendix D.

Video Storage And Display

In addition to the MRVS described above, the FY81 USPS/NOSC Statement of Work describes potential requirements for high-resolution displays and refresh memories for monochrome soft-copy image presentation. NOSC has been compiling informal notebooks containing literature related to potential candidate work station components; they may be used to satisfy future USPS work station requirements.

Memory Storage Technology

All present and planned future electronic mail systems require digital memory storage components at both the transmitting and the receiving sites for the image data and associated source, destination, and logistic information. Operational sites for INTELPOST and E-COM use memory to some extent for this purpose. For advanced concepts, a high daily volume of mail is expected to be transmitted through a large number of serving post offices (SPOs). Very large memories are required to store the daily information, since the sorting process may be accomplished only once per day before printing. Also the practices associated with merging, sorting, and controlling a multiplicity of output printing devices are complex. EDAC is also required to minimize the number of errors due to noise and dropped bits, which would otherwise destroy the accuracy or the quality of the transmitted information. NOSC is maintaining an informal set of files on newly emerging memory techniques and equipment.

DOCUMENTATION DELIVERABLES

A series of five interim technical reports was submitted to the USPS during the reporting period. These documents have been upgraded as required to reflect the status as of the end of the reporting period and are included herein as appendices A through E.

Memory Technology Assessment Report

An interim report on memory technology assessment was presented to the Postal Service in July 1981. That report has been upgraded to reflect the state of the art as of the end of April 1982 and is herein submitted as appendix A. It consists of a discussion of the types of memory applicable to the USPS requirements, including the various types of semiconductor random access memory (RAM), digital optical disk, conventional hard and soft discs, magnetic tape, and bubble memory. It discusses a variety of EDAC codes.

Image Acquisition Studies Report

This report includes a description of the work accomplished to upgrade the image capture and analysis system (ICAS) during the reporting period. It covers the mechanical as well as the hardware and software developments used in Scanner III. It includes some discussion of the evolution of 6-bit to 8-bit software, the introduction of the 8-bit A/D converter, and the addition of the ICAS interface to the hardware illumination corrector (HIC) and the hardware edge enhancer (HEE). The HIC and the HEE are discussed separately in much more detail in appendix E.

DoD Facsimile Data Compression Standard

NOSC provides technical support to the Naval Electronic Systems Command (NAVELEX, PME 110-21) for communications equipment design and acquisition. In this capacity, CE Winterbauer, NOSC Code 7323, contributes to US activities on the Tactical Digital Facsimile (TDF) and on the North Atlantic Treaty Organization (NATO) interoperability standard for communication systems. He has generated a technical report, NOSC TR 686, Digital Data Compression Algorithm Performance Comparisons, 30 April 1981. A condensed version of this report, prepared for the US Postal Service, is included as appendix C.

Preliminary System Architecture For A Modular Remote Video System

The results of the study of candidate architectures for a modular remote video system (MRVS) are contained in this report as appendix D. Included are discussions pertaining to work station design, image scan head design, human engineering considerations, digital display refresh, and the system input/output interfaces. System alternatives and a proposed development center are included.

Hardware Illumination Corrector And Hardware Edge Enhancer

Descriptions of the hardware illumination corrector (HIC) and the hardware edge enhancer (HEE) are contained in appendix E. Flow diagrams of the data and control paths for each equipment are given. Operational results to date are shown for the two equipments

newly added to ICAS. Samples of corrected and enhanced facsimile images are shown. A discussion of the error analysis shows the improvement due to the use of 8-bit as opposed to 6-bit pel values. Preliminary conclusions indicate that the HIC and HEE processes provide improved edge definition, particularly if more than two (bilevel) grey levels are used to display and/or print the image. Recommendations are made for using the NOSC selective filter plus some of the character repair algorithms of Delta Information Systems, Inc. to improve the compressibility of the images.

APPENDIX A

MEMORY TECHNOLOGY ASSESSMENT

by

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APPENDIX A CONTENTS

APPENDIX A ILLUSTRATIONS

APPENDIX A TABLES

ABSTRACT

This appendix provides an overview of available memory technologies that may be potential candidates for applications to very-large-volume image data bases. It also considers the memory and memory controller hardware and software needed to provide high-speed storage, sorting, and retrieval of facsimile documents as well as monochrome and color continuous-tone images. Applications of data compression to minimize the volume of stored imagery data and the methods of providing error detection and correction (EDAC) to insure essentially error-free retrieval (and subsequent transmission) are also considered.

The study indicates that optical digital disk recording, a technology scheduled to be available in the 1983 time frame, offers as a medium for storage of the actual images the advantages of optimum nonvolatility, error rate, speed of read and write, and physical volume.

The study also shows that because of its low access time, random access memory is the only feasible candidate memory technology for the linked list sorting process.

The remaining memory technologies can be considered as candidates for other applications in the acquisition, sorting, routing, and auditing of the image storage and retrieval processes.

INTRODUCTION

There is a rapidly increasing demand in both business and Government applications for document and image storage and retrieval systems. Although this discussion is directed toward US Postal Service (USPS) applications for advanced electronic mail systems, it encompasses almost identical requirements for very large document and image data bases required for military applications.

Major payoffs expected from advanced electronic mail systems include rapid delivery and a great reduction in the complexity of the sorting process. Mail collected from broad metropolitan and rural areas is brought to a sectional collection facility (SCF), where it is subjected to numerous machine and manual sorting stages (schemes). Mail for distant destinations is first sorted out by means of letter sorting machines (LSMs) with manual or optical character recognition (OCR) capability, then is rapidly shipped by air and surface carriers to other SCFs, where it is merged with local mail and further sorted into Postal Service route carrier sequences.

The concept of advanced electronic mail systems incorporates a large communication network, including satellite and common-carrier land links. Time division multiple access (TDMA) protocols allow each of the centers (estimated at possibly 150) to transmit in a "round robin" sequence to all others. Each center accepts and records all traffic data whose destination zip codes indicate local responsibility for ultimate delivery.

Message traffic is allowed to accumulate for some time before sorting and printing. The ideal accumulation period from the standpoint of sorting is 24 hours. By electronically sorting only once per delivery schedule before reducing the electronic messages to hard copy, physical merging of enveloped pieces into daily carrier sequences is not required.

Major engineering problems stem from the volume of data acquired during extended mail traffic storage periods. Figure A1 represents a hypothetical daily acquisition of letter mail in an area such as the lower Manhattan SCF, with advanced electronic mail systems in full operation. One million first class pieces would represent only one-half of the present daily traffic. If digitized as shown in the figure, approximately 2×10^{12} bits of image storage are required. In addition to the image memory, additional high-performance memory for the establishment and maintenance of the linked lists and sorting routines is required.

The following section describes the principal candidate memory technologies and their advantages and disadvantages for the various functions to be performed in advanced electronic mail systems.

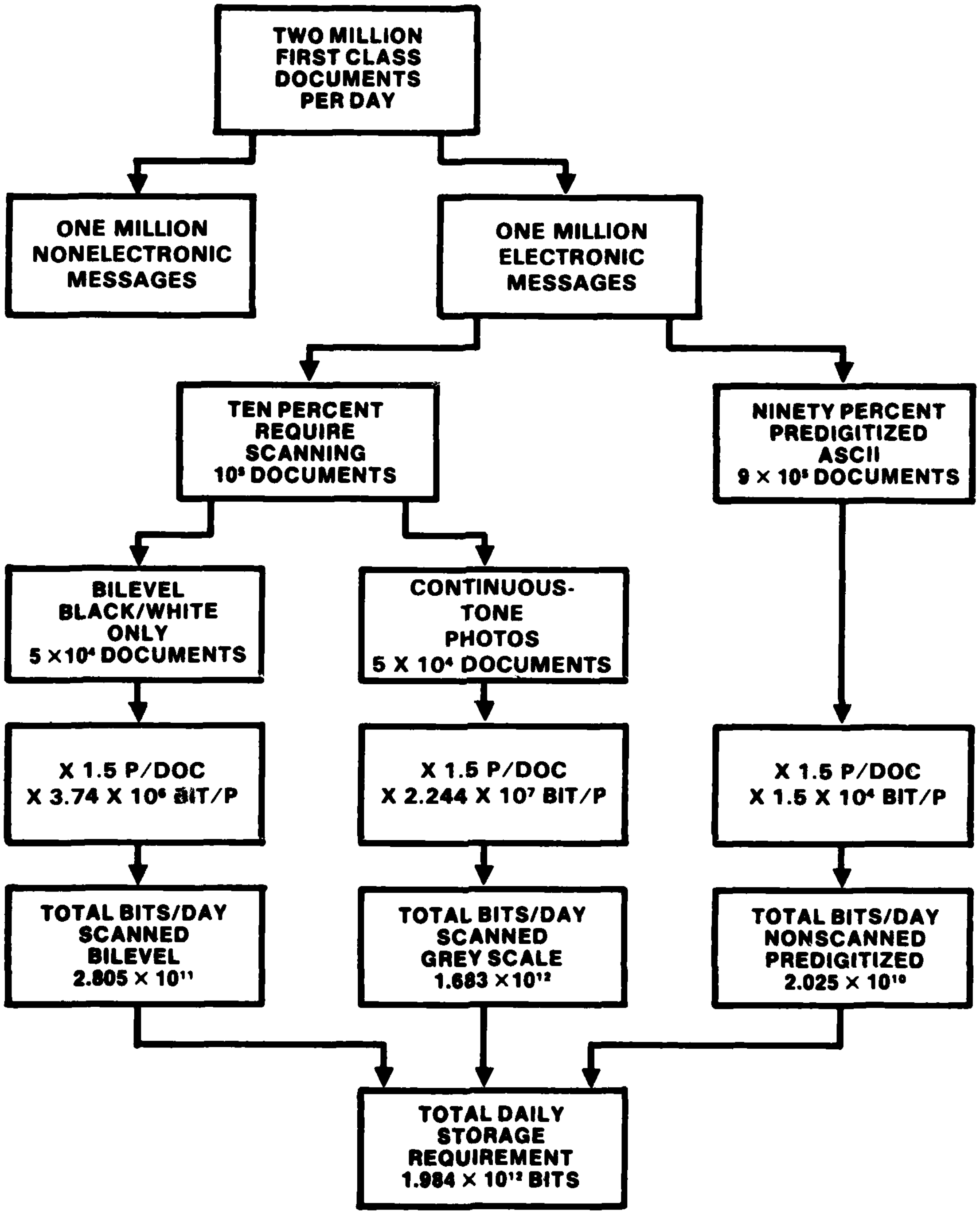


Figure A1. Center daily mail volume.

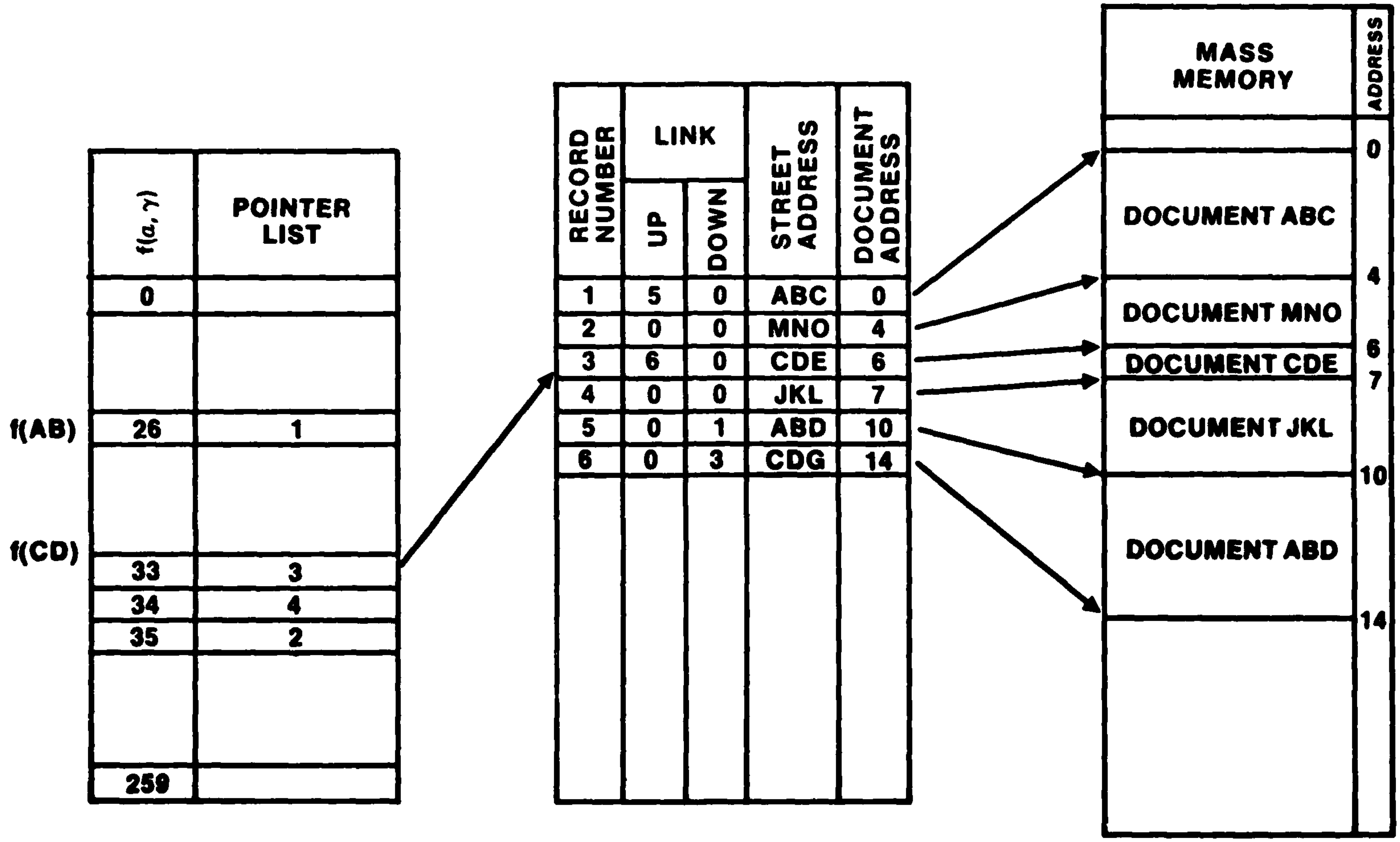
SYSTEM CONSIDERATIONS

With the anticipated mail volume, it is necessary to develop an architecture for the control, switching, storage, sorting, and dissemination of digitized facsimile and image document data for the USPS Electronic Computer Originated Mail (E-COM) and other advanced electronic mail system applications. This problem includes the memory technologies under review here as well as the control computer and switching architecture. There is a need for several types of memory for differing applications in this control architecture.

A very simplified diagram of three memory applications appears in figure A2. Of the three different memory lists shown, the pointer list at the left contains the principal master address categories into which the documents are to be sorted. This list can be relatively short and could be equivalent to the number of bins presently contained in an LSM. The list could also be equivalent to two consecutive LSM sorts, whereby the number of categories becomes the product of the number in the first sort times the number in the second sort.

The central memory list in the figure is the linked list, which is used very actively in the sorting process. Therefore it must be designed for very rapid access, comparison, modification, and storage. In this discussion, the 2-megabyte, 32-bit-word random access memory (RAM) in the Digital Equipment Corp. (DEC) VAX-11/780 is discussed as a candidate technology. Although the equipment requires 1800 nanoseconds to retrieve a specific word pair, the cache memory cycle time is 200 nanoseconds per word. Also the VAX-11/780 equipment provides the features of rapid access via direct memory address (DMA) channels to external peripherals such as 600-megabyte disk drives.

The third memory, at the right, is the storage location for the document data itself. This memory requires very high capacity and very high read/write speed. As mentioned above and shown in figure A1, the volume requirement might be up to 2×10^{12} bits per day. Recording rates of approximately 95 megabits per second may be required if continuous-tone 6-bit 8-1/2-inch by 11-inch documents scanned at 300 by 300 pels per inch at ten pages per second are acquired and/or transmitted.



$f(a, \gamma)$ is HASHING FUNCTION
COULD BE STREET ADDRESS: a = FIRST LETTER, γ = SECOND LETTER

Figure A2. Document storage and sorting.

VOLATILE SEMICONDUCTOR MEMORIES

Gordon Moore of Intel has predicted that the number of bits available on a single memory chip will double every year. And while "Moore's Law" may not be literally accurate, the trend of rapidly increasing semiconductor memory capacity continues. At least a dozen vendors are now offering 64-kilobit (64k) dynamic random access memories (RAMs) and most are developing 256k chips. Static 16k RAMs are being introduced and 64k static RAMs are expected to be available within a year. Pacing this trend is an ever growing demand for semiconductor memory products. It is estimated that by the end of this year 5 trillion bits will have been shipped and that by 1983 the yearly market for the 64k dynamic RAM alone will exceed $1 billion.

There are several classes of semiconductor memories. Dynamic RAMs, because of their high density, find application in large memory systems where their required refresh circuitry is not considered objectionable. Static RAMs are fabricated in either metal-oxide-semiconductor (MOS) or bipolar technologies. MOS static RAMs are preferred for small- to medium-size, medium-speed memories where the design simplicity which they allow is desirable. Since bipolar memories offer speed at the expense of high power and low density, they are usually found in small high-speed memories such as cache. An additional memory technology is the charge-coupled device (CCD).

DYNAMIC RAMS

A dynamic RAM memory cell consists of a metal-oxide semiconductor field-effect transistor (MOS FET) and a MOS capacitor. The charge on the capacitor defines the state of the memory cell. This simple structure makes dynamic RAMs the densest of semiconductor memories, and their per-bit power consumption is low. However, the memory must be refreshed periodically.

Most 16k and 64k dynamic RAMs (as well as the expected 256k RAM) are contained in 16-pin packages. Therefore, the address information must be multiplexed onto the chip. The memory cells are arranged in an array of rows and columns. To read or write into a particular cell, the row address of the cell is applied to the chip with the row address strobe (RAS), then the column address is applied with a column address strobe (CAS).

Each time a dynamic RAM memory cell is read, the charge content of the capacitor is altered. Therefore, dynamic RAMs are designed to refresh or recharge all previously charged capacitors in a particular row upon assertion of RAS. That is, each read or write operation is followed by a refresh period and, for this reason, the read or write cycle time is longer than the access time. Cycle time is the minimum time from one read or write operation to the next. Access time is the time required for the data to become available at the device output.

In addition to the charge loss suffered with a read operation, the charge on the capacitors decays with time, requiring that the entire memory be refreshed periodically. This is done by successively incrementing the row address and asserting RAS with each increment.

Manufacturers of 64k dynamic RAMs have differing views of refresh requirements. Motorola Mostek, and most of the Japanese IC makers (Hitachi, Mitsubishi, Toshiba, NEC, OKI, and Fujitsu) have attempted to maintain compatibility with the older 16k dynamic RAMs by specifying that each of 128 pairs of rows be refreshed every 2 milliseconds. This is done by configuring the memory as two 128-row by 256-column arrays. Each column is served by a sense amplifier, and a total of 512 sense amplifiers is required. The 7-bit refresh row address is cycled from 0 to 127 in 2 ms. Upon each RAS strobe, two rows of 256 cells each are refreshed. It is claimed that this arrangement allows shorter bit lines and thus lower capacitance per bit line and higher speed.

Texas Instruments, INMOS, National, and Fairchild have arranged the cells of their 64k RAMs as square arrays of 256 rows by 256 columns. There are 256 sense amplifiers, one for each column. Each of the 256 rows must be refreshed in 4 ms. Thus, an 8-bit row refresh address is required. It is asserted that, since this architecture requires 256 instead of 512 sense amplifiers, more area is allowed for memory cells and thus higher capacitance and charge per cell result in fewer soft errors. In addition, the smaller the number of sense amplifiers, the less power is used.

Despite their high density, power requirements for dynamic RAMs tend to be low. Standby power dissipation is generally between 20 and 30 milliwatts (mW) and operating power is around 125 mW.

The small cell size of the more dense dynamic RAMs causes concern over soft errors. These are thought to be caused by alpha particles (helium nuclei) from trace amounts of decaying radioactive material, mostly in the IC packaging material. These particles create electron-hole pairs that can reverse the charge state of the MOS capacitor. Although the mean time to fail for a single bit is estimated to be on the order of millions of years, a system with many bits of storage could fail more often. Efforts to reduce the susceptibility of dynamic RAMs to soft errors have been directed at increasing the capacitance of the MOS capacitors. Intel has upgraded their 64k dynamic RAM by boosting cell charge capacity to about 340 fC (femtocoulomb). Some manufacturers are also using protective coatings around the ICs themselves. There is speculation that dynamic RAMS will ultimately be limited in capacity by soft errors and that CMOS will become the dominant memory technology.

The 64k dynamic RAM is expected to become the most popular of integrated circuits. It will soon become the industry's first $1 billion part. At present, two US manufacturers, Motorola and Texas Instruments, are in volume production along with about six Japanese companies. Prices, driven by Japanese competition, have plummeted in recent months. Last year prices ranged from $30 to $100. Now they are near $8 for volume purchases. Next year, as supply expands to meet demand, further price reductions are predicted.

Texas Instruments offers a representative 64k dynamic RAM. It is organized as 64 536 words by one bit and is contained in a 16-pin package. Power consumption from a single 5-V supply is 125 mW operating and 17.5 mW standby. The part is available in three versions with access/cycle times of 150/280, 200/350, and 250/410 ns. The chip is fabricated by using MOS n-channel technology, and all inputs and outputs are TTL compatible.

The outlook for dynamic RAMs is for continued increase in capacity, at least to the 256k-bit level. This is the largest memory that can be contained in a 16-pin package if address data are multiplexed as two 8-bit bytes. IC vendors seem to be well on their way toward this goal; most of them have displayed 256k RAMs at recent trade shows and have announced that full-scale production will commence in 1983. In the US, Motorola seems to have the lead and will offer samples in early 1983.

Packaging is a problem faced by those companies pursuing 256k RAM development. The larger die size of the 256k chips developed to date has precluded the use of plastic packaging. Instead, the more expensive brazed ceramic packages are required. If the prices of 64k RAMs, which are packaged in plastic, remain low, then the 256k RAMs may not be cost competitive in the near future.

A special class of dynamic RAM contains some refresh circuitry on the chip. These are called pseudostatic RAMs. A row address counter is contained on the chip, but a strobe or clock must be provided for each row refresh. These are organized in 8-bit-wide configurations and are intended for smaller memories such as those used in microcomputer systems.

STATIC MOS RAMS

The static MOS RAM storage cell consists of a pair of n-MOS transistors cross-coupled to form a flip-flop circuit. Because of this, the state of the flip-flop is held actively and soft errors are not a problem. The newer static MOS RAMs are basically of two types: those which are fabricated in n-MOS throughout and those which employ an n-MOS cell structure and use complementary MOS (CMOS) for the peripheral circuitry. The latter are simply referred to as CMOS RAMs. Because the basic static RAM cell is more complex than the dynamic RAM, static RAMs are less dense; 16k bits is the largest size currently available. With the exception of the CMOS variety, static RAMs require more power per bit, but they offer the great advantage of not requiring refresh circuitry. Because there is no refresh operation with each read or write, the cycle times of static RAMs are only slightly greater than the access times. In terms of speed, some n-MOS static RAMs are approaching the access times of bipolar memories but with greater density and much less power. Since the newer CMOS RAMs, while featuring access times equivalent to n-MOS dynamic RAMs, require extremely low backup power, battery backup is feasible. (In fact, the prospect of high-density, low-cost RAMs with battery backup is a direct challenge to the bubble memory market, and this is said to have been influential in Texas Instruments' decision to drop their bubble product line.)

About 12 vendors sell 16k n-MOS static RAMs with access times around 55 ns. Most of these are organized as 16k x 1, cost about $50, and require 500/50 mW operating/standby power from a 5-V supply. There are lower-speed, low-cost alternatives--static RAMs with access times from 100 to 250 ns and prices from $8 to $20. Texas Instruments and others sell 4k static n-MOS RAMS. These are fast. Access times are near 35 ns and the price is less than $10.

Available now from Hitachi is a 16k (2k x 8) CMOS RAM with an access time of 120 ns. Power consumption is 180 mW active and 100 μW standby, and the cost is $85 in 100s. Other 16k CMOS RAMs are expected soon. These will have access times down to 55 ns, and some slower devices will consume as little as 1 μW of standby power.

Most static RAMs are bit-wide, ie a single bit is associated with each read or write operation. An increasing number of vendors are offering byte- or nibble-wide configurations. These attract small-memory designers because they increase modularity and allow memory expansion in smaller increments. However, byte-wide memories penalize designers with lower speed and higher power consumption.

Static MOS RAMs are expected to expand to 64k bits in capacity. Hitachi, Toshiba and Matsushita are said to be gearing up for production of 64k static RAMs. In fact, Toshiba has designed three different 64k static RAMs, two in CMOS and one in n-channel. As in the case of high-density dynamic RAMs, US manufacturers can expect keen competition from the Japanese in static RAMs.

BIPOLAR RAMS

Bipolar RAMs are available in two technologies: transistor-transistor logic (TTL) and emitter-coupled logic (ECL). The basic cell consists of cross-coupled bipolar transistors in a static configuration. Relative to other memories, TTL and ECL RAMs are the fastest but have the lowest density and the highest power consumption. TTL RAMs with access times of about 30 ns are being pushed hard by static MOS memories. However, ECL RAMs, with access times as low as 10 ns, continue to dominate where speed is the essential requirement. In both technologies, density is usually under 2k bits (in various configurations) and power dissipation is as high as 1 W per chip for ECL devices. Bipolar RAMs are found in high-speed special-purpose digital systems and in very-high-speed computer memories.

CCD MEMORY

A charge-coupled device (CCD) is essentially a large MOS transistor with a long channel and many gates between the source and drain. Charge can be trapped in potential wells beneath the gates by voltage applied to the gates and can be moved from gate to gate by the proper phasing of the gate

voltages. Thus, CCDs can be made to act as analog shift registers. CCD memories store digital information as the presence or absence of charge in potential wells. Unlike other forms of semiconductor memory they are serial in nature. They also have a minimum clocking rate to allow refresh amplifiers to purge thermally generated charge from empty potential wells.

The largest available CCD memory is the F264 CCD from Fairchild, a 64k device. It requires two input clocks and is organized as 16 recirculating shift registers of 4k bits each. The registers are randomly accessible but there is a latency time required to access a particular storage cell within a register. Minimum and maximum clock rates are 1 MHz and 5 MHz, respectively. The F264 CCD costs $12 in quantity.

CCD memories once offered a cost and density advantage over dynamic RAMs in some applications. With the arrival of 64k dynamic RAM, CCDs are no longer competitive. They have much longer access times, are more difficult to interface with, and are more expensive. Fairchild, a leader in CCD technology, will withdraw from the CCD memory market after selling its current inventory.

FUTURE RAM TECHNOLOGY

Silicon has historically dominated memory technology. A future alternative is Gallium Arsenide (GaAs). The electron mobility of GaAs exceeds that of silicon by about 5 times, and its parasitic ground capacitances are smaller. Thus GaAs promises faster memories, with access time on the order of 1 ns, and lower power consumption. Manufacturing difficulties abound, however, and the expected high cost of GaAs may limit it to military and signal-processing applications.

CHASSIS- AND BOARD-LEVEL DYNAMIC RAMS

Memory systems include, besides the memory chips themselves, other components such as interface and error detection and correction (EDAC) circuitry and, in the case of a chassis-level system, a physical enclosure with power supplies and cooling. These systems can be either purchased or designed and built in-house. The former option is often desirable since the design cost can be significant.

Add-in board-level memories are available for most computer systems from a variety of vendors. These memory boards are easy to use. To extend the memory capacity of a subject computer, they are simply inserted into the system backplane. To reduce costs, these boards are often populated either with 16k or partial 64k dynamic RAMs since there is usually no advantage to using a smaller-than-standard-size board.

Error detection and correction (EDAC) and battery backup enhance some memory boards. EDAC reduces memory system errors dramatically, but it incurs a storage and access time overhead. Despite this, EDAC is often found in

large memory systems and in those whose reliability is critical. Batteries now back up some static RAM boards. The advent of long-life lithium batteries and low- power CMOS RAMs has made this possible. However, these boards tend to be more expensive and have smaller memory capacity.

A 1-megabyte board for the VAX-11/780 is available from Texas Instruments. Last year, this board was sold for $9000, but the price is now $3295. It contains 288 32k dynamic RAMs (64k partials) for 1.125 megabytes. The additional 125 kilobytes are used for EDAC.

Complete memory systems are also available. Motorola offers a general-purpose memory system for $32 700. Called the System 3000, it contains a single 2-megabyte memory card with 288 64k dynamic RAMs as well as a power supply, mother board, and several other cards for interface and EDAC. The chassis can hold 15 additional 2-megabyte memory cards at $9000 each for a total capacity of 32 megabytes. This is a total of 32 megabytes for a price of $167 700 or $0.0006 per bit. An advantage offered by larger RAM systems such as these is the ability to read or write multibyte words in parallel, resulting in high data transfer rates. The System 3000 can read or write at 64 megabytes per second.

RAM COSTS

The price of RAM devices is fluid. It is a function of demand, grade of device, and quantity ordered. Most RAMs are available in two or three different access- and cycle-time specifications. "Partials" can also be purchased. These are devices with defects in one or more sections of cells. For instance, degraded 64k dynamic RAMs may be sold as 32k devices. In addition, the unit price is highly dependent upon the quantity and delivery schedule of devices required. Prices are adjusted frequently in response to market pressures. Much of this pressure comes from the Japanese, who seem determined to capture a large share of the worldwide RAM market. Table A1 is a summary of volatile memory types, chip and system availability, speed, and pricing.

	Capacity b=bit B=byte	Average Access Time	Average Data Rate (kbytes/s)	Cost $	Cost/Bit (millicents)	Mid-1982 Projected Capacity
RAM:						
Dynamic						
chip	64 kb	100-200 ns	250	8	12	256 kb
board-level system	1 MB	500 ns	2000	3295	40	8 MB
chasis-level sys.	2-8 MB	500 ns	64 000	8000-200 000	60	128 MB
Static						
n-MOS - chip	16 kb	50-250 ns		10-50	312	64 kb
CMOS - chip	16 kb	120 ns		85	600	64 kb
bipolar - chip	2 kb	10-50 ns		10	1000	2 kb
CCD						
chip	64 kb	13 ms	625	12	18	

Table A1. Volatile memory summary.

NONVOLATILE MEMORIES

FLOPPY DISKS

The floppy disk, originally conceived of as a replacement for punched cards and paper tape, represents a mature technology. (Shugart Assoc recently shipped their 500 000th unit). With some exceptions, technical progress is slow and price competition dominates.

A floppy disk system consists of a removable flexible disk, a disk drive, and a controller. Information is written onto or read from the disk via heads in contact with the disk's magnetic surface. The disks are either 5.25 inches (minifloppies) or 8 inches in diameter and rotate at 300 or 360 rpm. They can be single- or double-sided, although double-sided disks are becoming more popular. The industry standard IBM single-density 8-inch format provides 77 tracks per surface, 26 sectors per track, and 128 bytes per sector for a total of 256k bytes per surface. Other recording formats are offered with densities as high as 6000 bits per inch and 1.6M bytes per 8-inch disk. Floppies can be either soft sectored or hard sectored. Soft-sectored disks contain a single index hole denoting the beginning of the track, while hard-sectored disks have index holes for each sector. The trend is toward soft-sectored disks, and this is being accelerated by the recent introduction of single-chip controllers.

Average access time is the time required for the heads to traverse 1/3 of the tracks, settle, and be loaded, and for the disk to rotate 1/2 turn (latency time). For floppies this is typically 200 ms--a long time compared to the access times for hard disks. This, combined with a limited data capacity and low data transfer rates (typically around 60 kilobytes per second) tends to limit the floppy to serving as program and data storage for low-end microcomputers and as backup for hard disks. Prices for floppy disk drives are low. Shugart units range in price from $300 to $520 in volume.

A disk drive recently introduced by the Iomega Corp of Ogden, Utah, represents an apparent breakthrough in the state of the floppy disk art. The Alpha-10 drive stores 10 megabytes of formated data on one side of a single 8-inch disk. The linear bit density of 2[illegible] 000 bits per inch rivals that of many Winchester disk drives. The flexible disk, which is contained in a cartridge instead of the usual paper envelope, is stabilized very near the head by a unique design. As the disk rotates, it creates an airflow between itself and a special plate, called a Bernoulli plate. This airflow reduces the pressure between the two and brings the disk to within several mils of the plate while holding disk flutter to less than a mil. The read/write head then extends beyond the plate to within 10 microinches of the disk. The result is high recording densities and rates without significant disk wear. The compliance of the system lets contaminant particles pass between the head and disk without damage to either. Such an encounter can cause soft errors, which are then handled by an EDAC system capable of correcting burst errors of up to 4091 bits. The data rate is 1.13 megabytes per second and the average access

time is 35 ms. Because of its higher price, this drive will not compete with the conventional floppy drives; but it may provide an alternative to small Winchester drives with nonremovable media.

HARD MAGNETIC DISKS

Hard magnetic disk storage is perhaps the most exciting of the currently available nonvolatile memory technologies, in contrast to floppies and magnetic bubble memories. Performance gains are frequently announced and competition in this technology is fierce. There are 45 manufacturers on the growing list of those marketing hard disk drives. Demand, especially for the smaller 5.25-inch and 8-inch drives, exceeds supply. Although hard magnetic disks may eventually be replaced by optical disks for read/write nonvolatile storage, they are seen as a mainstream technology for at least the next 5 years.

Winchester technology is the foundation of these equipments. The first system to employ this technology was the IBM model 3340, introduced in 1973. It featured dual 30-megabyte drives, and this 30-30 configuration reminded some of a Winchester rifle. Thus the name, which has come to be synonymous with this type of hard magnetic disk drive. The essence of this technology is a sealed nonremovable head-disk assembly operating in a virtually contaminationfree environment in which the head "flies" above the disc on an air bearing of about 20 microns. There is no head-disk contact during disk rotation. When rotation slows, the low-mass heads land on a lubricated recording medium (usually a mylar-based ferric oxide) or on a special landing strip containing no data. The result is greatly improved reliability relative to older disk systems, and there is generally no routine maintenance. MTBF is usually 8000 hours and soft/hard bit error rates of $10^{-10}/10^{-12}$ are typical. In addition, the low-flying heads allow higher linear bit and track densities--on the order of 8000 bits per inch and 300 tracks per inch--and the simplicity of the fixed-disk design reduces system cost.

Two emerging rigid disk technologies are thin-film heads and plated thin-film media. Thin-film heads are made by photolithographic processes in which materials are deposited and shaped by techniques similar to those used in the semiconductor industry. These heads have smaller size and track width than are allowed by the machining operations used to manufacture conventional heads, enabling more precise control of critical dimensions and geometries. The results are greater recording densities and higher data rates. Thin-film heads are more expensive, however, and manufacturing problems have been encountered.

The second emerging technology is thin-film media. Conventional disk recording media consist of iron oxide particles dispersed in a binder and applied to an aluminum disk in a layer about 50 microinches thick. Thin-film media employ a continuous electroplated metallic film, usually of cobalt or nickel. Its thickness is a few microinches and can be precisely controlled. Greater recording densities can be achieved relative to the usual ferrite head

and oxide medium combination. In addition, thin-film disks are said to be no more expensive to produce than oxide-covered disks.

Winchester disk drives are found in three standard sizes: 5.25-inch, 8-inch, and 14-inch. The 5.25-inch and low-performance 8-inch drives are being integrated into microcomputer-based systems, while the larger capacity 8-inch and 14-inch drives are intended for minicomputers and mainframes. Also, a 10.25-inch nonstandard-size drive is offered by Fujitsu.

Of the three sizes, the 5.25-inch drive market is experiencing the most explosive growth. These devices have capacities as high as 16 megabytes (unformatted), average access times as low as 25 ms, and data rates of 500 to 1000 kilobytes per second. Generally, all three of these performance specifications are an order of magnitude improvement over the larger 8-inch floppy disk drives. Add to this a compact form factor that is identical to that of the standard 5.25-inch minifloppy, the use of standard interfaces, inherent reliability, and a cost of $1000-$2000, and it becomes clear why these smaller Winchesters are replacing floppy disk drives in many applications. However, a disadvantage common to all Winchesters is that the disks themselves are not removable. Thus, backup is usually required. This is most often provided by a separate floppy disk or tape unit. Market leaders in the 5.25-inch Winchester competition are Seagate Technology, International Memories, Inc, Shugart Assoc, Tandon Corp, and Irwin International.

An especially exciting product among the 5.25-inch Winchesters is the Irwin 510. It has a 10-megabyte formatted data capacity on a single disk with 25/40 ms average/max access time, 662 kilobyte/second data transfer rate, and an integral tape backup. All of this is contained in the industry-standard 3.25-inch by 5.75-inch by 8-inch minifloppy form factor. The tape subsystem uses 3M-type tape cartridges, which also have a formatted data capacity of 10 megabytes. Therefore, 100 percent backup can reside on a single cartridge. A complete dump takes under 4 minutes. The price is $1500 in quantity.

Capacities from 10 to 140 megabytes are offered by the 8-inch Winchesters. These units are used in microcomputer and minicomputer systems where their compactness, relative to the larger 14-inch drives, is desirable. In the middle of this performance spectrum, Quantum's Q 2000 delivers 40 megabytes from four disks at 542 kilobytes per second, with an average access time of 50 ms. The cost is $1800. At the high end, Ontrax's Series 8 contains 136 megabytes on 5 platters with an average access time of 25 ms and data rate of 1152 kilobytes per second. Other leaders in this market are IMI, Micropolis, Control Data Corp, and Fujitsu.

In a class by itself is the 10.25-inch Eagle from Fujitsu America. This product has 473.6 megabytes of storage with 18-ms average access time and transfers data at 1859 kilobytes per second. This capability rivals that of the 14-inch drives with less bulk and power dissipation and allows the Eagle to achieve compatibility with the higher performance minicomputers. The current cost is $8500 in quantity.

In the 14-inch disk drive market, several vendors sell products in the 500- to 700-megabyte range. Among these are Control Data Corp, Storage Technology Corp, Memorex, and ISS/Sperry/Univac. Two other companies, IBM and IBIS of Ogden, Utah, are introducing large capacity 14-inch disk drives, each using a different combination of technologies.

The IBM model 3380 writes data on conventional ferric-oxide media with thin film heads. This device stores 1.27 gigabytes on each of two spindles, for a total of 2.54 gigabytes. It transfers three megabytes per second of data with an average access time of 16 ms, thus is a leader in speed as well as capacity. The thin-film heads developed by IBM are responsible for this performance. Up to four 3380 units can be strung together for a total capacity of 10 gigabytes. An IBM 3880 Storage Control unit is required to interface the 3380 to various IBM processors. It can control up to two strings of four 3380s. Although announced in 1981, production problems have delayed initial shipments of the 3380.

IBIS has opted for a combination of thin-film media with proven ferrite heads for their 14-inch model 5000. This 5-gigabyte, 3-megabyte-per-second drive will compete directly with the IBM 3380 with which it is plug compatible. Its four head-disk assemblies are contained in a cabinet only 20% larger than that of the 3380. A separate control unit, model 5080, interfaces the 5000 with IBM mainframes. Initial deliveries are slated for 1983.

The future for rigid magnetic disk storage appears bright. Multiturn thin-film heads are being developed by Magnex Corp (San Jose), Applied Magnetics Corp (Goleta, CA), Hitachi, and IBM. Multiturn heads offer advantages over single-turn thin film heads. These include increased output signals, decreased writing current, and a reduction of magnetic loss in the magnetic yoke. Also being developed are improved actuator mechanisms that can reduce head positioning errors and thus allow higher track densities. It is predicted that recording densities will be pushed as high as 100 megabits per square inch by the mid-1980s.

Perhaps the most promising of magnetic disk concepts is called vertical recording: the creating of magnetic domains that are aligned perpendicular to the disk surface. The magnetic poles of the read/write head are on opposite sides of the disk. This configuration generates a highly localized magnetic field. Stray fields, which would tend to interfere with adjacent magnetic regions, are thus minimized. Japanese researchers have demonstrated 100 000 flux changes per inch on a sputtered thin film. This linear density exceeds that of the IBM 3380-type disk drives by an order of magnitude and even exceeds some linear densities achieved on optical disks. The Japanese are known to be actively researching vertical recording techniques. Several US companies, including IBM, are also involved.

MAGNETIC BUBBLE MEMORIES

Magnetic bubble memory technology has been described by Steve Weitzner, Electronic Products Magazine, as an "aging infant." It is a relatively old

but still immature technology, and prices have remained correspondingly high. There is incompatibility among competing designs and a lack of second sources. For these reasons, and because bubbles have presented difficulties in interface design, their reception has been cool and their use limited primarily to applications requiring nonvolatile storage in harsh environments or in portable equipment. Three manufacturers (Rockwell, Texas Instruments, and National) have recently dropped out of the commercial bubble market. This leaves Intel with most of the domestic market, challenged by Fujitsu and soon by Motorola. The cost of bubble memory is high--about $0.0017 per bit compared to minifloppies in the $0.00006-per-bit range. Recently, however, there have been indications that prices are beginning to fall, and interface problems are being addressed by the introduction of board-level memory systems featuring LSI controllers.

Since present bubble memory chips are bit-wide, a formatter is required for interface with an external data bus. Several other support chips are required as well. Access times are nearly 100 ms. This is fast relative to floppies but orders of magnitude slower than semiconductor memory. Data rates of about 100 kilobits per second are much slower than those of either floppy or Winchester disk drives.

The largest bubble memory available is Intel's 1M-bit part; a 4M-bit chip is scheduled for late 1982. Despite National's recent withdrawal from the market, its 256-kilobit memory, the NBM 2256, is representative. This device stores data in magnetic domains or bubbles that move under metal patterns deposited in the chip. The bubbles are arranged in 282 loops of 1024 bits each. Twenty of the 282 loops are redundant, 6 are used for error checking, and the remaining 256 contain data. The bubbles are moved in a step-like fashion around their respective loops by a magnetic field applied once each 10 μs. This field is generated by a current through on-chip coils from an off-chip driver. A page of data consists of one bit from each of the 256 loops, so there are 1024 pages. To read a page of data, the loops are rotated until the desired page is opposite an output track, also composed of bubbles. The page is replicated onto the output track, and the contents are then clocked past an output detector. The process of writing a page is similar.

Fujitsu makes bubble memory cassette subsystems. The 128 kilobyte cassette system, including cassette, holder, and control/interface card, sells for $2760. Designed to replace small floppy disk systems, they can be used for test equipment, numerical controls, and other applications.

A multibus-compatible bubble memory board is offered by Intel. It contains four 1-megabit memories for 512 kilobytes and includes a memory controller with EDAC. The price is $3585 in small quantities.

Intel will introduce a 4-megabit device with a full complement of support chips in early 1983. It is expected that this larger capacity will result in a significant reduction in the cost of bubble memory.

MAGNETIC TAPE

While not new, magnetic tape still offers the highest capacity, lowest cost removable storage presently available. With the trend toward Winchester disk drives (which are nonremovable) there is renewed interest in the magnetic tape, especially as backup for the disks. The great disadvantage of tape, of course, is its very long access time, on the order of minutes. The uses of tape include archival storage, system backup, transportation of data from system to system and data storage in instrumentation systems. Today there are three categories of magnetic tape: 1/4-inch-wide tape cartridges used in small computer systems, 1/2-inch-wide tape for medium and large scale computers and 1- and 2-inch-wide tape used in instrumentation. Tape drives are either of the start/stop or streaming variety.

The replacement of floppy disk drives by Winchesters in low-end systems has prompted a need for removable storage in these systems. In many cases requiring 10 to 20 megabytes of storage, this removable storage is being provided by 1/4-inch 3M-type cartridges. Streaming 1/4-inch digital cartridge drives in this capacity range are around $500 and a 75-megabyte capacity drive sells for about $2000. While the tape cartridges themselves are standardized, recording formats differ widely and transportability is usually possible only between like drives.

A standard for years has been IBM-compatible 1/2-inch phase-encoded tape recorded at 1600 bits per inch per track. Data transfer rate is 160 kilobytes per second at 100 inches per second (ips) and a 2400-foot reel can contain 37 megabytes of formatted data. Streaming 1/2-inch tape drives can cost as little as $3000.

Higher-density 1/2-inch tape formats are available but they do not allow the wide transportability of IBM-compatible tapes. Storage Technology Corporation offers a 1/2-inch tape drive which utilizes group-coded recording (GCR) technology. Recording density is 6250 bits per inch, which allows a maximum of 180 megabytes to be stored on a 2400-foot reel. The maximum transfer rate at 125 ips is 780 kilobytes per second.

The streaming technique of data recording has allowed the cost of 1/4-inch and 1/2-inch tape drives to be reduced significantly. Streamers write data blocks and interrecord gaps on the fly; they do not have to be capable of stopping suddenly at the end of each data block within the interrecord gap as do the older start/stop drives. At the end of the last data block written, the streamer's read/write head passes the interrecord gap and enters the next data block space as it decelerates. It must then back up to the interrecord gap. This requires a relatively long time (about one second). If the data rate of the host device is matched to that of the streamer, it is possible to achieve higher continuous throughput rates than those of a comparable start/stop drive. But if the streamer has to stop and start frequently while waiting on the host, then the throughput can be less because longer wait times are required to accelerate and decelerate. For these reasons, multiple speeds are often available on streaming drives.

In a class by themselves are high-density digital tape recorders for instrumentation such as those from Honeywell, Bell & Howell, and others. Two machines from Bell & Howell are particularly impressive. The 3700 HI-D Laboratory Recorder can store 10-1/2 gigabytes of formatted data on 28 tracks of a 9200-foot reel of 1-inch tape with a density of 27.4 kilobits per inch. The larger System 600 records 36 gigabytes of formatted data on 84 tracks (72 for data, 11 for EDAC and 1 for search) of 2-inch tape 9200 feet long at a density of 44 kilobytes per inch per track. The data rate of 3700 HI-D is 11.5 megabytes per second while that of the System 600 can be as high as 450 megabytes per second. Costs are approximately $100 000 for the 3700 HD and $1.5 million for the System 600. Both machines use Bell & Howell's version of enhanced non-return-to-zero (E-NRZ) recording format on each data track. An odd parity bit is injected after every 7 serial data bits and the 2nd, 3rd, 6th and 7th bits of the group of 7 data bits are inverted. This scheme minimizes the low-frequency component of the data stream, and the parity bit assures a transition every 8 bits. A unique 40-bit sync word is written after each group of 80 8-bit words. Its purpose is to separate the data into 560-bit blocks and to synchronize the circuits that remove skew between different tracks of output data. To accommodate this overhead, data are recorded or read at a rate 17/14 higher than the input or output rates. Thus, data are recorded at a constant rate with no stopping for interrecord gaps.

Extensive EDAC is standard on the System 600, whose bit error rate (BER) is specified at 10^{-8}. EDAC is an option on the 3700-HD. With it the BER is improved from 10^{-6} in the standard configuration to 10^{-10}. With EDAC, however, the 3700-HD capacity is reduced since 4 of the 28 tracks are unavailable for data. The EDAC methodology is similar on both systems. It involves the parity bits recorded simultaneously after every 7 data bits across all data tracks as well as parity bits for simultaneous data bits that are recorded serially on dedicated parity tracks. This two-dimensional parity encoding is combined with interleaving of the 8-bit data/parity words to allow isolated errors, simultaneous errors on several tracks, and burst errors to be detected and corrected. This scheme is claimed to be so effective that an entire track can be rendered inoperative without significantly affecting the BER.

One characteristic of all tape systems is long access time. Tapes do not enjoy the intrinsic organization of disks, where data are addressed by the particular track on which they are written. To locate a tape file or record, the tape must be searched; ie the tape is wound or rewound while file marks are counted. Some systems provide a higher search speed for the purpose while others search at the read/write speed. If data are distributed uniformly over a tape (or disk) and if the probability of being at a particular point on a tape (or track on a disk) is also uniform, then the average length of tape (or number of tracks) to be traversed to reach the desired data is one-third the total tape length (or numbered tracks). For a 1/2-inch tape system that contains a standard 2400-foot reel and whose search speed is 100 ips, the average access time is 1.6 minutes.

Another characteristic of the tape medium itself is very low storage cost per bit. For instance, a 1/2-inch, 2400-foot reel of certified digital tape costs about $20. In the standard 1600-bit-per-inch IBM-compatible format, it can store 37 megabytes at a cost of about $0.000003 per bit! Formats with much higher density are also possible. Tape systems require periodic maintenance (including head replacement), however, and the cost of the system itself can be significant. The costs of some representative magnetic tape systems are listed in table A2.

OPTICAL DIGITAL DISK

High-density disk recording is a rapidly emerging technology. Two types of video disks have reached the consumer market for television video playback. These are the Magnavox/Philips/Sylvania/Philco Magnavision laser-optical disk and the RCA/Zenith/Sears SelectaVision capacitance electronic disk (CED). A third contender, the Matsushita/JVC/GE video high-density (VHD) system is expected to be available in a few months. None of these approaches is suited for USPS applications, since they all require time-consuming preparation of master disks in order to produce high-volume duplicate copies. Also, the bandwidth is inadequate for the record and playback speeds required in this study. A third drawback is that the analog methods of recording do not provide a suitable form for data compression or EDAC.

A very-wide-band digital optical-disk digital recorder/playback system is being developed at RCA, Camden. This system uses either a water-cooled gas laser or a solid-state laser diode as a source. Extremely high density digital recording (1.25 μm between tracks having bits on 0.67 μm centers) allows the recording of 10^{11} bits per disk. EDAC provides an error rate improvement from 10^{-8} (without EDAC) to 10^{-10}. Almost any error rate can be achieved by selecting the proper encoding scheme.

The recording medium is a plastic trilayer 12-inch-diameter disk approximately 0.25 inch thick. The trilayer consists of a thin metal layer and a reflector layer separated by a transparent dielectric. The thickness of the dielectric layer and the optical density of the metal layer are chosen to provide almost complete cancellation of the reflected light from the surface of the metal. A sturdy substrate and a transparent overcoat provide durability for the disk during handling and storage.

To record, the disk is mounted on a precision spindle and turned at either a constant angular velocity or a constant linear track velocity. For simplicity, the former mode is preferred. A precisely controlled modulated laser beam is focused on the metallic layer of the disk. Either spiral or circular tracks can be generated by controlling the position of the track mirror, which is mounted on a motor-driven translation stage and precisely controlled by a galvanometer mirror (the dither track servo).

	Capacity b=bit B=byte	Average Access Time	Average Data Rate (kbytes/s)	Cost $	Cost/Bit (millicents)	Mid-1982 Projected Capacity
Bubble						
chips	1 Mb	7 ms	10	380	37	4 MB
board level sys	0.5 MB		50	3585	87	2 MB
Floppy						
5.25 & 8 inches	0.25–1.6 MB	200–400 ms	60	200–500	4	
Winchester						
5.25 inches	3-12 MB	25-100 ms	500-900	1000	1.7	40 MB
8 inches	5-136 MB	20-50 ms	600-1200	1000-3000	0.7	400 MB
14 inches	30-1260 MB	20-50 ms	600-3000	2000-100000	0.4	2.5 MB
Tape						
1/4-inch	75 MB/600 feet	1.3 min	24	2000/30*	3/0.005*	
1/2-inch	37 MB/2400 feet	1.3 min	160	3000/20*	1/0.006*	
1-inch	10.5 GB/9200 feet	1.6 min	11 500	100k/100*	0.1/0.0001*	
2-inch	36 GB/9200 feet	1.6 min	450 000	1.5M/200*	4/0.0004*	
Optical Disk						
wideband	93 GB/side	3.0 s	400 000	1.5M/20*	0.6/0.000 02*	9313 GB

*system/medium

Table A2. Nonvolatile memory summary.

When full power from the laser strikes the metallic surface, the temperature of the metal is raised above the melting point and a pit opening in the layer is formed. The pits are slightly elliptical and have dimensions of approximately 0.3 μm by 0.2 μm. This recording density allows a raw recording capacity of 1.2×10^{11} bits over the usable surface of the single-sided disk.

During playback, reduced laser power is focused on the tracks. Where no pits have been written, only very low reflected energy is received by the read photo sensor. Where pits have been made during the writing process, high reflective energy from the exposed mirror surface is detected by the read sensor.

In this manner, very-wide-bandwidth recording and reproduction is accomplished. Digital rates up to 50 megabits per second are possible by using delay modulation (DM). DM is an improved code, similar to Miller code, in which the dc component has been removed. Block coding for EDAC adds overhead to the signal data so that, at present, about 7.5×10^{10} data bits can be written on a disk.

RCA is designing an eight-channel parallel recording system using a 1-watt argon laser and a beam splitter. The beam splitter divides the beam into eight individually modulatable beams, which are focused simultaneously onto eight parallel data tracks. The net recording rate is thereby increased to about 320 megabits per second. Readout is accomplished by positioning the laser (at reduced power) over the same eight tracks and sensing the reflected data through eight photodetectors.

RCA has preliminary designs for a 10^{13}-bit "jukebox" reader that has a capacity of 100 disks and a 10^{14}-bit mass memory system that would contain 10 jukeboxes.

ERROR DETECTION AND CORRECTION

Advances in theory, application, and available hardware for EDAC are emerging very rapidly. Because of the increased dependence on the accuracy of large volumes of high-speed data received from storage or transmission sources, error detection logic and software correction provisions are being incorporated into a growing number of equipments and systems.

Errors occur in a number of ways both in and between electronic systems. Transmission errors consist of bit and/or burst errors. Bit errors consist of either single bits that are reversed because of very high frequency noise or inadvertent dropouts of one or a few bits. Burst errors come from long-duration interference patterns during transmission, which interrupt a considerable sequence of digital data and cause the data to be lost and uninterpretable. There are also system errors, which come from electronic logic errors, power transients, and address calculation errors within the memory storage and retrieval system.

Furthermore, memory errors occur when memory devices fail in the "stuck at 0" or "stuck at 1" mode and continue to give erroneous outputs regardless of the intended data to be stored. With the advent of submicron geometry for integrated circuits, there is also a new failure mode called "radiation turnover." This type of "soft" error results from bombardment of the electronic microcircuits by alpha particles, forcing a change in the logic state. These failures produce random errors rather than the consistent errors caused by stuck bits.

Two hardware devices exist for the correction of 16-bit memory words on dynamic random access memory (DRAM) cards. These are the Texas Instruments 74LS630 and the Advanced Micro Devices AM2960. Both devices provide the capability to detect and correct one error per 16-bit memory word. These devices can also flag 2-bit errors and allow the system to be halted and restarted. With the 16 data bits supported by the devices, associated overhead requires an additional 6 bits per word for the EDAC code. The use of 22 bits to provide single-error detection and correction for 16 bits is defined as a (22, 16) coding system.

The AM2960 device can also be used in systems having 32 or 64 bits. Two or four devices can be used for 32- and 64-bit memory systems, respectively. For a 32-bit system, 7 bits of EDAC code are required. For the 64-bit memory word using four AM2960s, the storage overhead becomes 8 bits per 64-bit word. It can be seen that the relative ratio of overhead required decreases as the width of the word increases. The 6 bits required to provide the correction and detection codes for the 16-bit word represents a 37.5% overhead. Similarly, the overhead for the 32-bit and 64-bit EDAC codes represents only 21.9% and 12.5%, respectively.

In addition to the reduction of overhead required for error correcting codes, the trend in memory architecture is toward wider words. For example the DEC VAX-11/780 computer utilizes 32-bit data words but the memory is organized to access 64 bits at a time. Undoubtedly, the VAX-11/780 utilizes a set of devices such as the AM2960 for EDAC at the board level.

ERROR DETECTION AND CORRECTION CODES

In the process of correcting errors in data signals, two principal types of codes are employed: block codes and tree codes. Block codes have been in use longer than tree codes. The theory, techniques, and application of block codes are reasonably well understood but are still advancing. Most of the block code techniques employed utilize a subset known as linear block codes. Block codes usually divide the data into regular lengths of message data, then add a code to the end of the information message. These added bits are called redundant digits; and when added to the actual message, they produce a code word which is transmitted over a channel. It is received and presented to the decoder, whose task it is to verify that the message portion of the text was properly received. In the event that erroneous data due to noise have been accepted, the decoder must provide the proper correction of the bits and present this to the destination as a valid message.

Tree codes are more generally used for message transmissions of long or indefinite length. The data in tree codes are not broken up into blocks but are continually fed to a decoder that operates on the data stream to produce a corrected data output set. Convolutional codes are a subset of tree codes, so called because the flow diagram is most conveniently described by means of a tree graph. Convolutional codes are best applied to the situations where burst errors are almost nonexistent and the bit error rate is reasonably low.

LINEAR BLOCK CODES

Linear block codes form the major subset of all block codes used for EDAC. Within the linear block code subset are a number of very familiar coding techniques. The most popular types of codes are the following:

Hamming (RW Hamming)

Golay (MJE Golay)

Reed-Muller (IS Reed & DE Muller)

Bose-Chaudhuri-Hocquenghem (BCH) (RC Bose,
DK Ray-Chaudhuri, and A Hocquenghem)

Reed-Solomon (IS Reed & G Solomon)

Fire (P Fire)

Orchard

Concatenated

Some of the above codes are subsets of other types but were generated by a different set of design rules. A brief descriptive abstract of the distinctive feature of each of the above codes follows.

Hamming formulated the concept of "distance" and "weight." The Hamming distance is the minimum number of positions in a code in which the elements are different. In subtracting one code word from another in linear block codes, the difference must also be a code word. Therefore, the difference between two code vectors must be equal to the code weight of another vector in linear codes. Hamming codes are parity check codes and are also in the class of cyclic codes. A code set allowing the detection and correction of a single bit error requires that for the transmission of an "m" bit code, "k" check bits be added to the code word such that $2^k \geqslant m + k + 1$. Table A3 summarizes this relationship.

m	k
1	2
2-4	3
5-11	4
12-26	5
27-57	6

Table A3. Single-error-correcting code check bit table.

In 1950-54, Golay searched for and found a "perfect" code (23/12) [or by adding to it an overall parity bit (24/12)], which will correct all patterns of three or fewer errors. These are cyclic codes.

Reed-Muller codes are formed from the vector product of two or more vectors. They lend themselves to majority vote decoding and are noted for being easy to decode.

Bose-Chaudhuri-Hocquenghem (BCH) is the most powerful and extensive code class in existence to date. The BCH codes form a large class of cyclic codes, first defined as binary codes and later generalized to codes in pm, where p is a prime integer. The algebra for formulating and manipulating these codes and locating errors has been highly formalized.

Reed-Solomon codes are a subset of BCH codes that are more effective against clustered errors than against random errors. It is particularly effective for byte-oriented data and a transmission channel having infrequent burst errors (causing several errors per byte) and relatively few bytes in error.

Fire codes (developed by Philip Fire), like Reed-Solomon codes, are best adapted for infrequent burst errors such as might be encountered on reading from magnetic disk recordings. These codes are product codes of several polynomials and are discussed in some detail in references A1 and A2. Advanced Micro Devices, Inc, has designed the AM Z8065 burst-error processor (BEP) in a large scale integration (LSI) MOS circuit to provide hardware implementation of these codes, which can have up to 56 check bits and can accommodate a burst error up to 11 bits long in a data stream 585 442 bits in length.

Orchard codes are a new concept in EDAC and have not yet achieved hardware form. These block codes use diagonal geometry in the code vector matrix as well as the conventional row-column strategies now in everyday use. These orchard codes, so named for the row-column-diagonal symmetry of organization, were conceived by the Analytical Engine Works, Glendale, California, and are said to approach a minimum redundancy rate of one bit per word.

Concatenated codes are combinations of any sets of codes used in tandem. These codes use an outer and inner encoder and decoder in the generation of the stored or transmitted messages. Data encoded by the outer encoder (which, for instance, may recover many single-bit errors) are encoded again by the inner encoder (which may withstand infrequent burst errors). The inner and outer decoders provide the correction capabilities to reinstate the correct values of the originally transmitted message.

A1. Johnson, RC, Three Ways of Correcting Erroneous Data, Electronics, p 121, 5 May 1981

A2. Maniar, M, and K Rallapalli, Fire Codes on Custom Chip Clean Up Hard Disk Data, Electronics, p 122, 5 May 1981

EXAMPLES OF EDAC

<u>A Hamming Code.</u> An example of a single-error-correcting Hamming code is shown in figure A3. For this code, three parity bits P_0, P_1, and P_2

	Bit Position					
	6	5	4	3	2	1
Message	A	B	P_2	C	P_1	P_0
0	0	0	0	0	0	0
1	0	0	0	1	1	1
2	0	1	1	0	0	1
3	0	1	1	1	1	0
4	1	0	1	0	1	0
5	1	0	1	1	0	1
6	1	1	0	0	1	1
7	1	1	0	1	0	0

Assume a received message: 1 0 1 0 0 1

The P' received parity bits are generated as follows:

bit pos		data rcvd		parity		output bit	
1, 3, 5	=	1, 0, 0	=	Odd	=	$P_0' = 1$	
2, 3, 6	=	0, 0, 1	=	Odd	=	$P_1' = 1$	Binary three
4, 5, 6	=	1, 0, 1	=	Even	=	$P_2' = 0$	

This indicates that bit position three is in error and must be inverted. The correct message is therefore 1 0 1 1 0 1, which is the code for a transmitted message "5."

Figure A3. Single-error-correcting code example.

have been added to the three data bits, A, B, and C. P_0 is the even parity bit for bit positions 1, 3, and 5 of the encoded word. P_1 provides parity for bit positions 2, 3, and 6. P_2 gives parity bit information for bit positions 4, 5, and 6.

On receipt of an incoming code, the parity bits P_2', P_1' and P_0' are generated from the appropriate incoming bits. In the example, the incoming parity bits generated are $P_2' = 0$, $P_1' = 1$, and $P_0' = 1$. For this parity structure, the parity code word $P_2'P_1'P_0' = 011 = 3$ indicates that bit position 3 is in error and must be reversed. Using the corrected code word, bits 6, 5, and 3 give an actual incoming message of "5."

<u>A Cyclic Code.</u> A more complex example is shown in figures A4, A5 and A6. For this example, three pairs of octal (perhaps ASCII) characters are to be transmitted. The eighteen bits are combined into a single bit-stream and prepared for transmission, least significant bit first. An irreducible primitive polynomial is selected as a divisor for the message bit-stream and logical division modulo 2 (same as addition and multiplication) is performed on the data stream. Six zeros are appended to the end of the message and the division is carried out through the entire 24-bit encoded block. The remainder, in this case 1101, is added to the last six bits of the message and the block is then transmitted.

Upon receipt, the incoming block is again divided by the same polynomial. If there are no errors in the communication channel and the encoding and decoding systems, then the remainder will be zero and the message is immediately usable as is. This is shown in figure A4.

If a remainder exists, as in figure A5, the remainder is entered as an address of a lookup table. For each of the possible 24 single-bit errors there exists a discrete remainder. The lookup table defines the location of each specific error. It also senses whether the bit error is in the message field portion of the block or in the appended 6-bit check bit area. No correction process is necessary if the error is in the 6-bit remainder field because that field is not part of the message and will not be used further. The second example in figure A6 shows an error in the check-bit area. Errors located in the message field must be corrected before the data is output from the decoder.

The remainder field can also detect double bit errors, but cannot correct them. Such errors are flagged and a signal is available to request a retry or halt command to the host processor or controller. See the first example of figure A6.

Table A4 shows a partially populated table of the lookup values for the polynomial chosen. With this message length and this polynomial, if the ninth bit of the code word is in error, the remainder will be 10101.

<u>Interleaving.</u> Another technique useful for EDAC is interleaving. Interleaving is accomplished by loading one of two identical buffers, row by

```
      45              21              16         Characters
   100 101         010 001         001 110       to be
   Character 1     Character 2     Character 3   transmitted

   X^6+X^5+1 = 1 100 001                         Polynomial divisor

18-bit character message  :  6 appended zeros

   101 001 100 010 011 100 000 000               Initial code word
   110 000 1
    11 001 000
    11 000 01
         1 010 010
         1 100 001
           110 011 011
           110 000 1
                11 111 100
                11 000 01
                   111 110 000
                   110 000 1
                     1 110 100
                     1 100 001
                        10 101 000
                        11 000 01
                         1 101 010
                         1 100 001
                             1 011               Remainder

   101 001 100 010 011 100 001 011               Received code word
   110 000 100
    11 001 000
    11 000 01
         1 010 010
         1 100 001
           110 011 011
           110 000 1
                11 111 100
                11 000 01
                   111 110 000
                   110 000 1
                     1 110 101
                     1 100 001
                        10 100 011
                        11 000 01
                         1 100 001
                         1 100 001
                                 0               Remainder = 0; Message OK
```

Figure A4. Properly generated and received code word.

```
0                                                 Bit received in error
101 001 100 010 011 100 001 011                   Transmitted word
  1 100 001
    101 101 010
    110 000 1
     11 101 110
     11 000 01
        101 100 011
        110 000 1
         11 100 111
         11 000 01
            100 101 100
            110 000 1
             10 101 000
             11 000 01
              1 101 010
              1 100 001
                  1 011 001
                  1 100 001
                    111 000 011
                    110 000 1
                      1 000 111
                      1 100 001
                        100 110                   Error remainder

          1                                       Bit received in error
101 001 100 010 011 100 001 011                   Transmitted word
110 000 1
 11 001 001
 11 000 01
      1 011 010
      1 100 001
        111 011 011
        110 000 1
          1 011 111
          1 100 001
            111 110 100
            110 000 1
              1 110 000
              1 100 001
                 10 001 001
                 11 000 01
                  1 001 011
                  1 100 001
                    101 010 011
                    110 000 1
                     11 010 111
                     11 000 01
                         10 101                   Error remainder
```

Figure A5. Single-bit error remainders from decoder.

```
         11                                  Bits received in error
101 001 100 010 011 100 001 011              Transmitted word
110 000 1
 11 001 011
 11 000 01
      1 001 010
      1 100 001
        101 011 011
        110 000 1
         11 011 111
         11 000 01
             11 101 100
             11 000 01
                101 110 001
                110 111 1
                 11 001 101
                 11 000 01
                      1 111 011
                      1 100 001
                         11 010         Error remainder

                            1           Bit received in error
101 001 100 010 011 100 001 011         Transmitted word
110 000 1
 11 001 000
 11 000 01
      1 010 010
      1 100 001
        110 011 011
        110 000 1
             11 111 100
             11 000 01
                111 110 001
                110 000 1
                  1 110 101
                  1 100 001
                     10 100 111
                     11 000 01
                      1 100 101
                      1 100 001
                            100              Error remainder
```

Figure A6. Double-bit error and code group error.

Remainder	Action
0	Accept message. transmission OK
100 110	First (left-hand) bit erroneous, invert it.
010 101	Ninth (from left) bit erroneous, invert it.
000 100	Twenty-first bit erroneous, not in message field, use message portion as is.
011 010	Two or more bits in error, flag uncorrectable errors and halt.

Table A4. Partial lookup table for error correction values.

row, at the transmitter or data source as shown in figure A7a. When the buffer is full, data are extracted from the buffer column by column and transmitted. During the extraction the alternate buffer is being filled row by row.

At the receiver, one of two identical buffers is loaded with the serially received data, column by column. When the buffer is full, the message data are drawn from the buffer row by row and are now back in their original sequence (see figure A7b).

The two identical pairs of buffers at the transmitter or source and the destination are used in "ping pong" fashion for the data. While one buffer is being loaded at the source and destination, the other pair is being read out.

The advantage to interleaving is the ability to disperse burst errors into single-bit errors. For convolutional decoders and for some types of block decoders, correction of more numerous single-bit errors may be simpler than correcting a single burst.

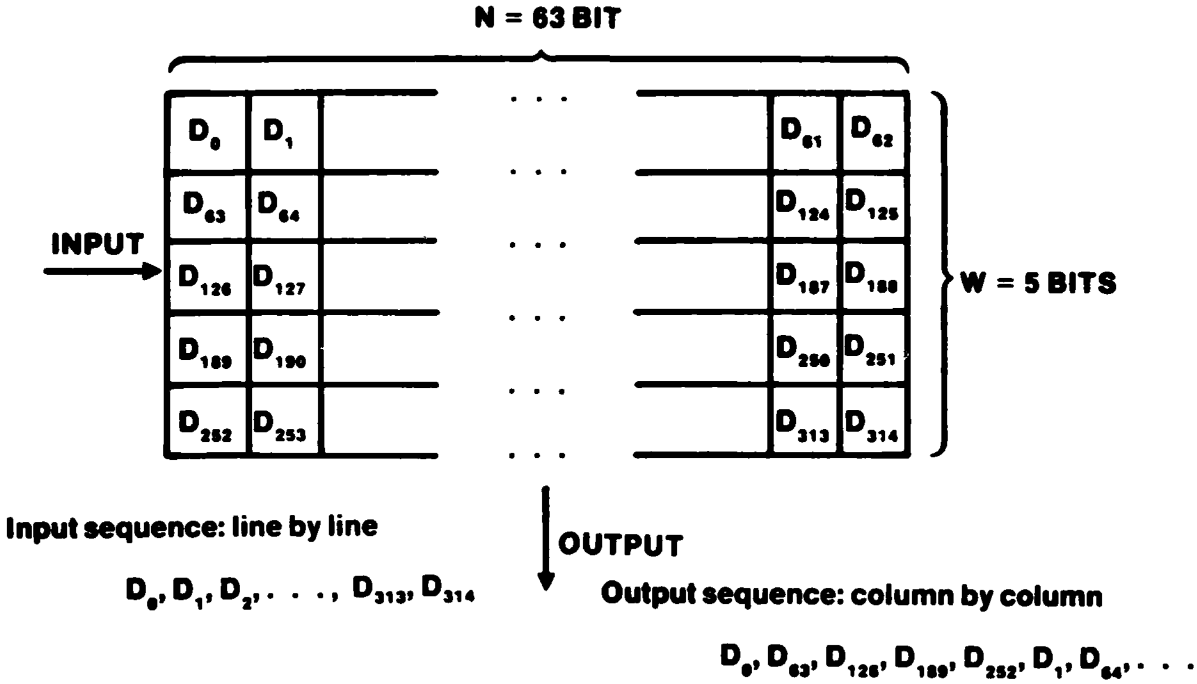


Figure A7a. Interleaving of data.

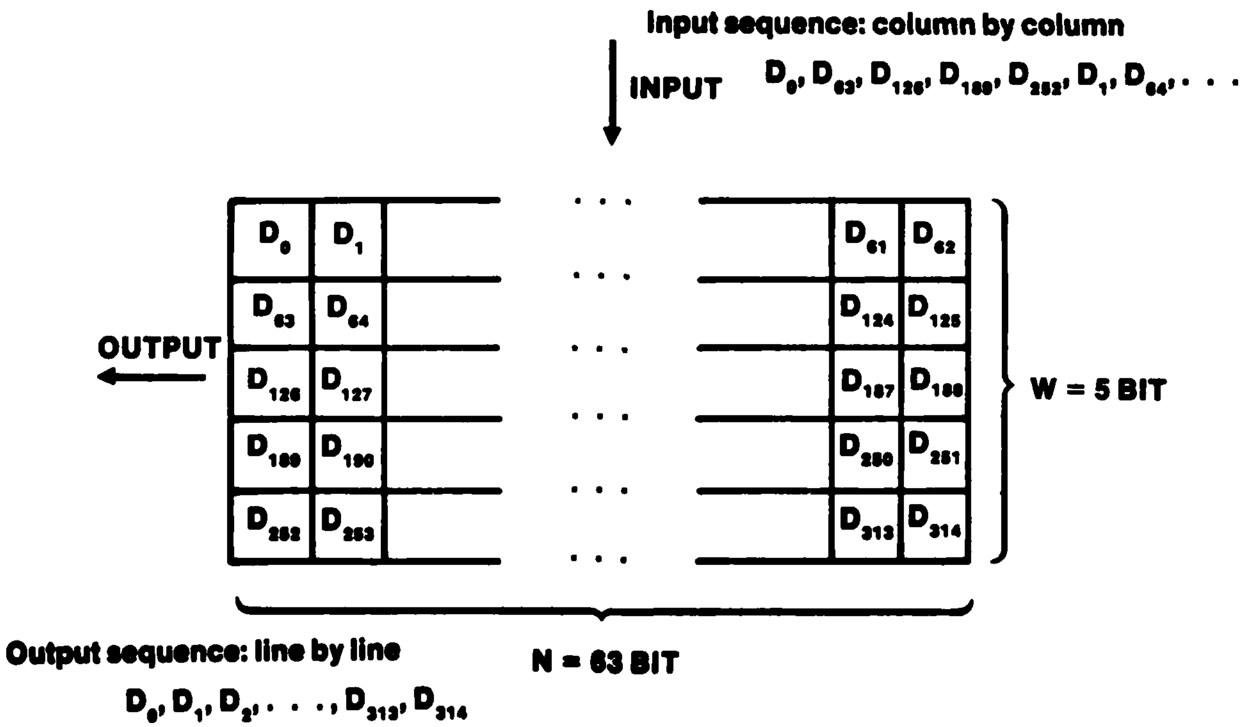


Figure A7b. Deinterleaving of data.

A STRAWMAN LETTER SORTING ARCHITECTURE

SYSTEM DESCRIPTION

Figure A8 is an example of an architecture that can handle the advanced electronic mail sorting problem with today's technology. The basic assumption is that the system will input data for 12 hours and then print data for 12 hours. Data come into the system over telephone lines, on magnetic tape, on computer disks, and/or via a satellite link. Each of these different inputs is attached to a Format/Buffer Unit (FBU). The FBUs will check the incoming message and, where possible, correct any errors. Any uncorrectable error will cause the message to be flagged for human handling. In general, the incoming data will be in a format different from that required by advanced electronic mail systems; therefore the FBUs will be responsible for changing the format.

As each message comes in, the street address, city, state, and zip code are copied. A hash algorithm (probably different for each field) is then run on these data; and the results, in combination with the length of the message, are used to make a prefix that is attached to the message. The prefix is also sent to the computers, which locate a sufficiently large space in bulk storage to accommodate the message. The bulk storage controller is then given the message size, and the message is placed on a data bus to bulk storage.

The incoming data are generally received at a slower rate than the potential bandwidth of future advanced electronic mail systems would allow. Each FBU will have two buffer memories, one to be filled at a low rate while the other is emptied at a high rate. An example of a bus that can handle the required data rate is the Hyper Net™.

Bulk storage devices have a built-in delay, called inertia, between the command to store data and the time they are able to do so. Therefore, an "inertialess" electronic buffer will be located between the data bus and the bulk storage devices, preventing the data bus from being required to wait for the bulk storage device setup before delivering the data.

During the setup delay, the storage location of the message is added to the prefix in the computer. While the message is being stored, the computer uses the state, city, and street address to determine the correct zip code, which is compared with the received zip code. A disagreement causes the message to be flagged for human processing. Otherwise, the computer determines whether the message is local or is to be sent to a remote station (probably by satellite). If the message is not local, its prefix is placed in a queue with the prefixes of other messages bound for the same zip code. Local messages are further processed to determine by which carrier route and where in the route sequence the message should be delivered. The message prefix is then inserted into the appropriate carrier queue/sequence for later printing.

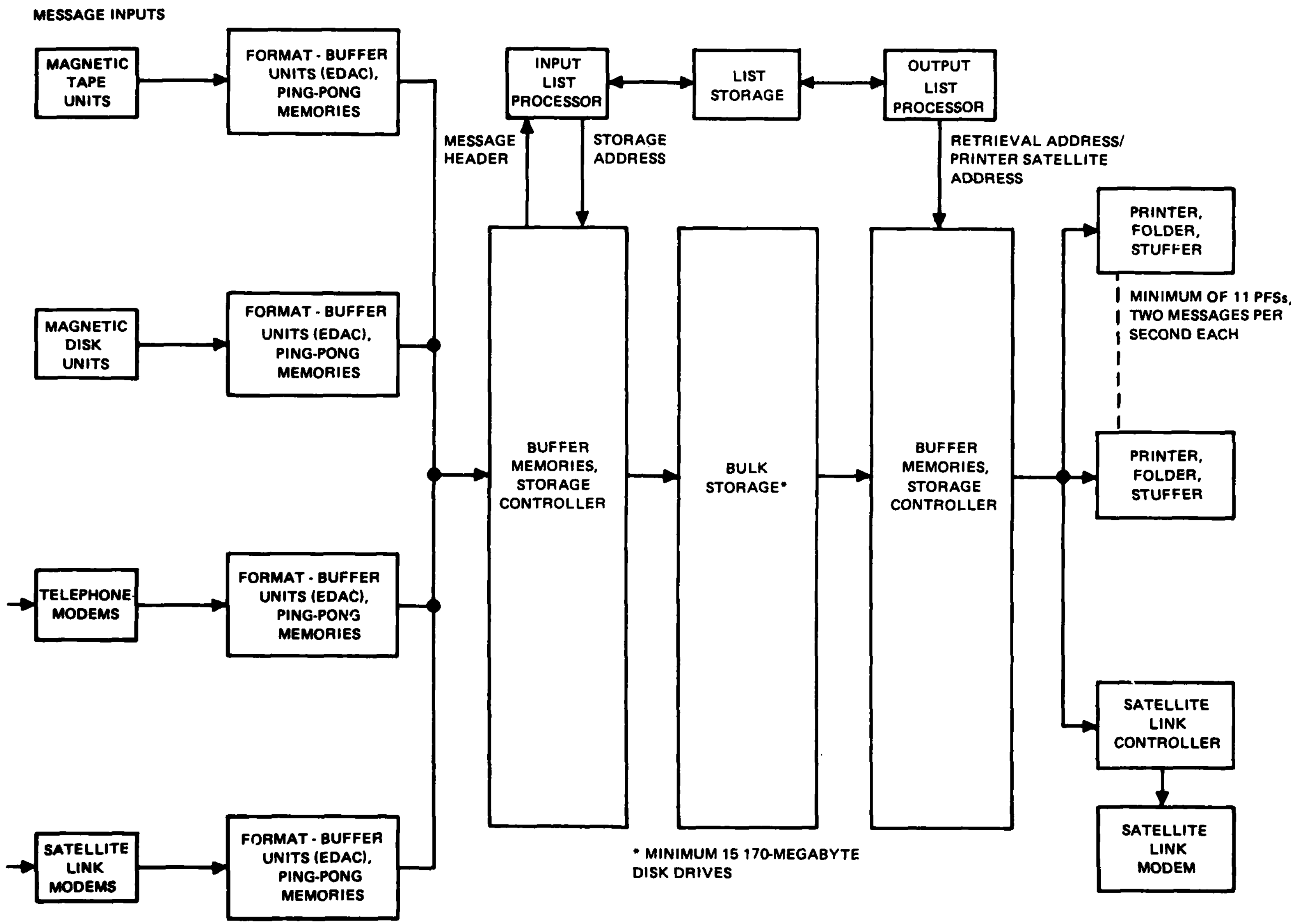


Figure A8. Electronic mail sorting system.

During the second twelve hours the system prints the contents of the carrier queues in the sequence in which the carrier will deliver them. When a message has been released from the system (either by local printing or by transmission via the remote channel/satellite link), the system returns that message area to the list of bulk storage available for use.

On the output side of the system, buffers are provided to remove the delays caused by the bulk storage device inertia so that the output bus can be utilized efficiently. The output bus delivers the data to the printers and the satellite link controller. The satellite link controller strips off the prefix and reformats the data to the form required by the satellite link. The output system notes the prefix, prints the message, folds the paper, and inserts it into an envelope. The former concept of placing extra advertising material and a preprinted return-addressed envelope in the same package with the printed message becomes very difficult because the printed messages are sorted by carrier delivery sequence and not by message originator.

SOFTWARE FUNCTIONS

The activities discussed in the system description section are accomplished by the computers, which perform the routing and scheduling functions with the aid of linked lists (discussed shortly). A list of states, probably addressed by hashing to save time, contains entries pointing to a list of cities in that state. The list of cities is also to be addressed by hashing. Each city list contains a pointer to a list of streets for that city (addressed by hashing). Each list of streets points to a list of numbers on that street. Each list of numbers has two pointers, one for the zip code for that address and one for the carrier route in which it belongs (and probably the location within the route sequence). In the system description section, mention was made of placing the prefixes on queues. This was only symbolic. Each nonlocal zip code and carrier route identifier has a pointer that points to the first entry in its queue. Each entry in a queue is actually referenced by two pointers, one to the physical location of the prefix and the other to the next entry in the queue.

The list of bulk storage area is called a free list. Each entry in the free list consists of three parameters: a pointer indicating the location of the beginning of a free area in bulk storage, a word indicating the size of the free area, and a pointer to the next entry in the free list. BLISS, BCPL, and C are compiler languages that handle linked-list processing programs nicely. Linked lists are used very heavily in compiler writing and in operating systems.

STORAGE REQUIREMENTS

In the first section we assumed that data would be input for 12 hours. Assuming that there are one million messages in that time, the system will have to handle an average of 24 messages each second or about one message

every 41 milliseconds. Present-day computers such as the DEC VAX could process a prefix as described above with no problem. Two processors with shared storage could be used for redundancy. Individually, the prefixes are small, but a million of them require substantial storage. Since different lists also require substantial storage, the shared storage will probably consist of two disk drives. The data rate on the bus would be approximately 600 000 bits per second. Electronic Computer Originated Mail (E-COM) is a near-term subset of advanced electronic mail systems that provides for the electronic transport, switching, sorting, printing, and final carrier delivery of message data in ASCII format. For this subset (assuming that the average message is 1.5 pages long with an average of 1.5×10^4 bits per page), 20 disk drives, each with a 170-Mbyte capacity, will store one day's message traffic with some room for redundancy to allow for defects on the disks. For scanned image data, a mass storage medium such as the digital optical disk or the Bell & Howell 600 storage medium will be required.

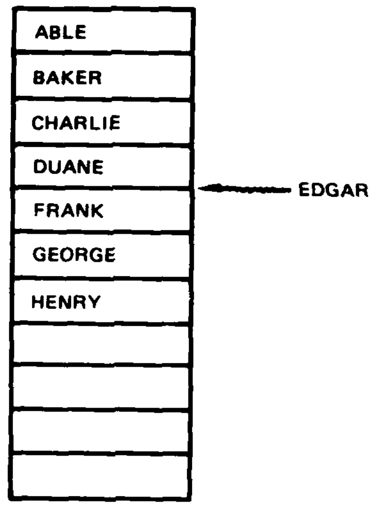
LINKED LISTS

A list is a group of data (names, numbers, etc) ordered in some fashion (alphabetical, numerical, etc). Computer programmers store data as lists of various lengths and logical attributes. Computer hardware addresses its memory as one long linear list. Compilers perform the bookkeeping to allow programmers to generate other types of data structures easily.

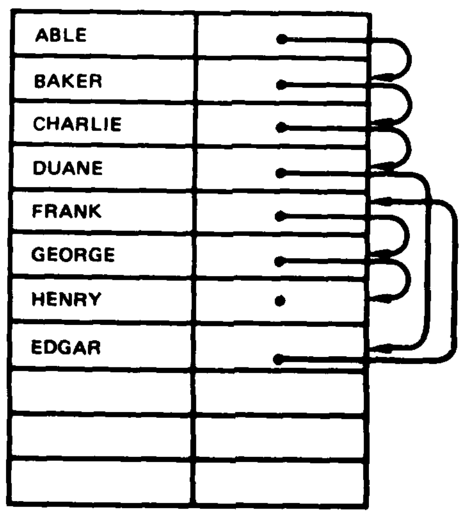
In a computer, each separate entry occupies a word of memory. Figure A9a shows a list of names. To insert Edgar's name alphabetically, Henry, George, and Frank must first be physically moved down one space. This procedure is acceptable if the list is short. If the list is long, the time necessary to move the items can become prohibitive. With today's technology, memory is cheap. A technique called linked lists spends memory to save processing time. Figure A9b shows the same list done with links. Two memory cells are assigned to each item. One cell contains the item itself and the other cell contains the location of the next item. When Edgar is entered into the list, Duane's link is corrected to point to Edgar and Edgar's link is set to point to Frank. If Frank is deleted from the list, then Edgar's pointer is adjusted to point to George. After many additions and deletions the list appears to be scrambled when moving sequentially through memory. Following the pointers, however, the list will be traversed in the proper sequence. Linked lists are sometimes constructed with more than one pointer per item. If processing time is critical, each item may have two pointers, one to the following item and one to the preceding item. In cases where the items are long, two or more words per item may be required. Where the items appear on more than one list, each item would appear in memory only once and each list would contain linkage pointers as well as a pointer to the item itself.

HASHING FUNCTION

Sometimes it is necessary to store a list that is mostly empty. For



(a)



(b)

Figure A9. Example of list sorting process.

example, a list of all English-language 6-letter words is shorter (by several orders of magnitude) than the list of all possible words that could be constructed of six letters from the English alphabet. A list long enough to accommodate the latter would be very wasteful of memory if it were necessary to accommodate only the former. One way to store such data is to allocate enough space in memory to hold all of the items to be stored and to construct an algorithm that it is hoped will yield a unique location for each item within the allocated area.

This type of procedure is called hashing. For example, by assigning a number value to each letter (A equals 0, B equals 1, ..., Z equals 25), a word can be considered to be a number to the base 26. Thus, a six letter word would represent a number between zero and 308 915 786 (which can be represented in a 32-bit binary word). For this example, assuming we need to store no more than 2000 6-letter words, we assign 2000 32-bit words for storing the data. To store a word we first convert the letters to the equivalent binary number, save it, divide it by 2000, multiply the remainder by 2000, use the result as an address into the storage area, and store the actual data value there.

This algorithm, an example of one hashing technique, in summary is:

1. Convert the word to a base-26 number
2. Convert the result to binary
3. Divide by the size of the storage area and multiply the remainder by the size of the storage area
4. Use the result as an address

There are many more hashing algorithms in use. This technique has the disadvantage that it does not always give a unique address. It has the advantages that the English word is now in a form that takes only 32 bits to store rather than the 48 bits that the ASCII representation takes and that it is faster than many other techniques for accessing an existing entry.

VAX-11/780

Because of increased user sophistication and improved price performance characteristics, demand for 32-bit super minicomputers has increased significantly. A current market leader is DEC with its VAX-11/730, 11/750, and 11/780 machines. The VAX-11/780 was introduced in 1977; and its younger brother, the 11/750, in 1980. The newer 11/730 was released in 1982. The 11/750 incorporates gate array logic. Its performance is roughly 60% of that of the 11/780 at about half the cost. The VAX systems are expected to be standards of the 1980s much as the PDP-11s were for the 1970s. The following is an overview of the VAX-11/780 capabilities. Figure A10 is a pictorial overview.

The VAX-11/780 is a high-performance 32-bit computer with a multiprogramming/multiuser virtual memory operating system. The virtual address space spans 4 gigabytes (2^{32}) and is organized into pages of 256 bytes each. Of the 4 gigabytes of virtual memory, 500 megabytes are allocated for user programs and data. The physical address space is much smaller than 500 megabytes but this is transparent to the programmer since the operating system swaps data between main memory and disk as needed.

The VAX-11/780 central processor unit (CPU) executes 244 microprogrammed instructions with cycle times of 200 ns. It has 16 general-purpose 32-bit registers, 32 interrupt priority levels, an 8k-byte cache memory and an 8-byte instruction buffer. The instruction set supports nine addressing modes and operates on integer, floating point, character, and packed decimal strings and bit fields. The cache memory is write-through; that is, the same data is simultaneously written to the main memory while it is being written to the cache. Since instructions are buffered, the CPU does not have to slow down while waiting for the write-through to take place.

The interface between the system operator and the CPU is via a microcomputer-based console system. It contains a console terminal and a floppy disk system and provides system initialization, bootstrapping, and system diagnostics.

VAX-11/780 main memory consists of one or two memory controllers, each supporting sixteen 256k-byte array cards composed of 16k-bit, 600-ns MOS RAMs. The maximum main memory capacity with two controllers is therefore eight megabytes. Data are read and written as 64-bit quad words with an additional byte used for error detection and correction. Read/write cycle times are 800/1400 ns for quad words. Masked write operations involving a subset of the quad word take longer since this requires a read-modify-write cycle. With the optional second memory controller, interleaving of memory is possible for increased throughput.

The VAX-11/780 main memory communicates with the CPU and other system elements over the synchronous backplane interconnect (SBI). This bus has a 32-bit-wide data path and shares the same 200-ns cycle time as the CPU. Data

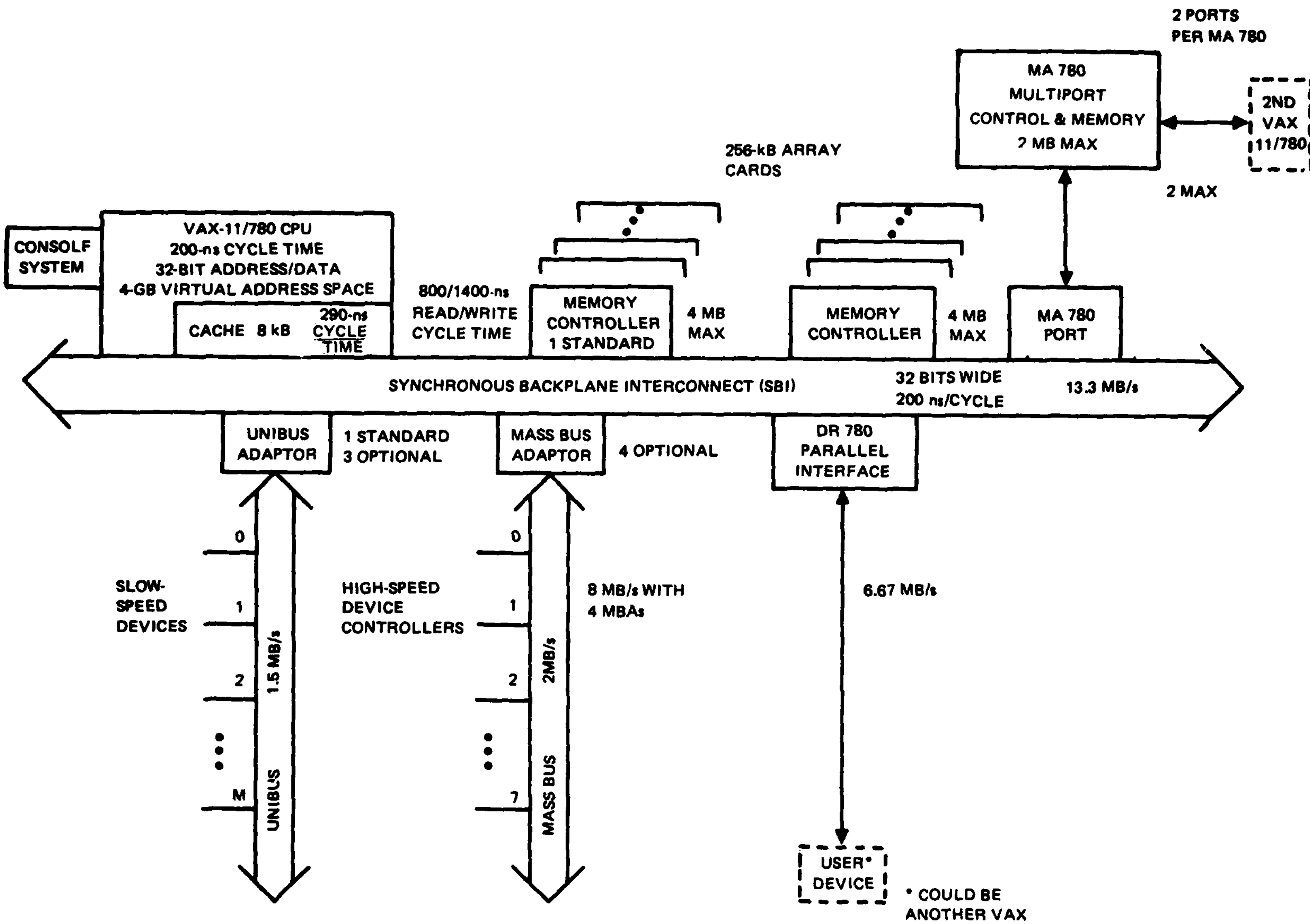


Figure A10. VAX-11/780 overview.

throughput on the SBI is calculated as follows. Since data can be written to or fetched from memory in 8-byte quad words, one SBI cycle is required to transfer the address and 2 more cycles are required for data. Thus the data rate is:

2/3 x 4 bytes/cycle x 5 megacycles/second = 13.3 megabytes/second.

Low-speed devices such as CRTs or line printers are attached to the UNIBUS. The UNIBUS adaptor provides an interface between the UNIBUS and the SBI. The UNIBUS cable is 16 data bits wide and is capable of a maximum throughput of 1.5 megabytes per second. One UNIBUS adaptor is standard with the VAX-11/780.

Controllers for high-speed devices such as disks and tape drives are linked by the MASSBUS. This is also 16 data bits wide. A maximum of eight device controllers are allowed on the MASSBUS. The MASSBUS adaptor interfaces the MASSBUS with the SBI and up to four may optionally be included in the system. The maximum data rate per MASSBUS adaptor is 2 megabytes per second. With four MASSBUS adaptors and two memory controllers, a DMA (direct memory access) rate of 8 megabytes per second can be supported.

DEC has recently introduced two interesting MASSBUS peripherals: the RP07 Winchester disk drive with associated RH780 controller and the TU78 tape drive. The disk drive stores 516 megabytes of formatted data with an access time of 31 milliseconds and a transfer rate of 2.2 megabytes per second. A single RH780 controller with eight RP07 drives allows over 4 gigabytes of on-line storage. The controller is a multiport device, so that two VAX processors can share the disk data base. The TU78 tape drive uses the increasingly popular group coded recording (GCR) ANSI standard 6250-bit-per-inch format. A single 2400-foot reel of tape can contain up to 145 megabytes. The maximum transfer rate is 780 kilobytes/second at 125 inches/second.

DMA is provided by the optional DR780 parallel interface. This allows a high-speed 32-bit data path between system main memory and a user device and is a means for directly linking two VAX systems together. Throughput is highly dependent upon system environment. With two memory controllers and when neither the CPU nor any peripherals are accessing memory, the maximum memory read or write rate is 7.5 megabytes/second.

In addition to main memory, the MA780 provides 2 megabytes of multiport memory, which can be shared by other VAX systems. Two MA780s are optional, with two ports each. Thus, the total system RAM can be 12 megabytes.

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APPENDIX B

IMAGE ACQUISITION STUDIES

by

LA Wise
RW Basinger
PC Grossnickle
RJ Wagar

Code 7323

JR Tower

RCA, Camden, NJ

APPENDIX B CONTENTS

APPENDIX B ILLUSTRATIONS

APPENDIX B ILLUSTRATIONS (cont)

APPENDIX B TABLES

ABSTRACT

This appendix describes the FY81 efforts at NOSC in the general area of scanner technology. The major areas in which this effort is directed are imagers, illumination source, analog signal processing, A/D conversion, and digital signal processing. The major accomplishments were the fabrication of a new scanner test unit, Scanner III (which is capable of supporting a variety of scanners or imaging devices and associated electronics), and the procurement of an illumination corrector and an edge enhancer which are designed to operate at 20 megapels per second.

The imaging devices discussed are the Fairchild CCD 143, a 2048-element linear array, and the RCA TC1262--a 748-element by 96-line time-delay and integration (TDI) imager. The CCD 143 is operational on Scanner III at a speed of about 1.5 pages per second. At this rate the imager is operating at about 17% of saturation, which is marginally sufficient for digitizing images to 6 bits or 8 bits. It is hoped that tests on the TC1262 will show that, by integrating each line many times, the full dynamic range of the imager can be utilized at the present illumination level at faster page rates.

Tests on the illumination corrector and edge enhancer indicate that there is a need to do some kind of digital filtering on the image data before performing the edge enhancement algorithm. If there is any imbalance between the two output channels of the CCD 143 imager, the resulting "odd even" differences are amplified by the algorithm. If there is no odd-even noise in the image data, the algorithm does perform well.

Detailed characterizations of four TRW TDC 1007J 8-bit A/D converters were made. Within the limits of the methodology, they showed very good uniformity from one device to another. It was noticed that there is a several-millivolt shift in the buffer amplifiers used in the support circuitry. This shift has a cycle of several minutes and should not cause problems during scanning operations.

IMAGE ACQUISITION

During the first half of FY81, NOSC fabricated a new test bed for use in testing and characterizing imaging systems, new imagers, and both analog and digital processing components and subsystems. The test fixture, Scanner III, is shown in figure B1. It provides an optical table with a rotating drum and light source for scanning documents. In the 19-inch rack-mount sections below the table are an indicator panel, an electronics card cage, and a set of power supplies. This unit was designed so that different imaging systems or components of imaging systems can be tested on Scanner III by installing a set of electronics cards for each different imager in the card cage and mounting the imager and lens combination on the optical table. Currently, the CCD 143 imager and its driver electronics are installed and operating. Soon to be tested is the RCA TDI imager TC1262, with its associated electronics.

SCANNER III

Scanner I, the small-drum test bed (SDTB) designed for image acquisition applications, consisted of an optical bench 14 inches wide by 32 inches long. A small drum having a diameter of 3.82 inches (12-inch circumference) was fitted with a shaft encoder providing quadrature voltage levels at spatial increments of 0.00143 inch. Illumination was provided by a quartz-iodide line-filament lamp mounted under the table with the output reflected onto the drum surface from two mirrors through a narrow slit in the bench surface. The A/D converter and line drivers were located in a "doghouse" above the bench surface.

For a number of reasons, this table became only marginally adequate for NOSC requirements. When the USPS printer and paper-handling equipment (PPHE) was designed, the paper transport drum was fabricated with a circumference of 40.96 inches. This provided 0.005-inch increments (200 pels per inch resolution) with the 8192 pulses per revolution of the shaft encoder. In addition to the benefits of compatibility, the larger diameter drum was also desirable for NOSC area and TDI imager studies. The NOSC Scanner I could not accommodate the larger drum without a major redesign.

Scanner II, the large-drum test bed (LDTB), was designed and fabricated with a 13.038-inch diameter drum, 9 inches wide. The height of the drum centerline remained the same. The table area was expanded to 45 inches long by 14 inches wide. The increased length accommodated somewhat lower scan densities (100 pels per inch) with some lenses, but still required an extender for some longer focal length lenses at low scan densities. Slit-aperture fluorescent lamps directly adjacent to the drum surface replaced the lossy two-mirror quartz-iodide lamp system. As in the SDTB, the lamp power supply was located under the optical table, making repairs very cumbersome.

Figure B1. Scanner III.

A decision was made by USPS and NOSC to fabricate a scanner drum assembly for use as government furnished equipment (GFE) for characterization of the time-delay and integration (TDI) imager by RCA, Princeton, NJ. A third-generation scanner table was designed, fabricated, and delivered for this purpose. The axis of the 13.038-inch drum was raised from 2.5 to 7 inches to provide space for the support electronics surrounding the TDI imaging device. No "doghouse" for electronics was supplied since RCA was furnishing the support electronics.

In 1981, a decision was made to fabricate a duplicate of the scanner table design sent to RCA, for use at NOSC. A sturdy rolling table having standard rack-mount bays was procured to accommodate the expanded support electronics required to condition and digitize video signal data from the four TDI imager output channels. Line drivers for parallel transmission of up to four 8-bit pel data streams are required. Control electronics for Scanner III are much superior to the those of the former units. Control storage registers for the selection of first line, first pel, number of pels per line, and number of lines per image have been added. These can be loaded from the Tektronix 4054 terminal.

ILLUMINATION

The illumination source chosen for use on Scanner III is a dual-lamp fluorescent source that uses a 19 kHz ac power supply. The two fluorescent tubes are housed in enclosures that include light guides and plastic cylindrical Fresnel lenses to concentrate the light output into a relatively narrow line across the surface of the drum. This is essentially the same illumination source as is used on the EDM Scanner in operation at USPS R&D Labs in Rockville, MD. This source is shown in figure B2 mounted on Scanner III.

It was intended that this illumination source would satisfy several objectives, namely to provide increased uniformity over the source used at NOSC on previous scanners, to reduce phosphor component migrations within the tubes due to dc excitation, to provide higher overall illuminance levels on the drum surface, and to provide either a flat or photopic spectral response over the spectral range of 400 to 700 nm when used with a CCD-type imager. All of these objectives have been met, but there are still shortcomings, which will be discussed here.

The illumination falling on the drum surface is shown to have about an 18% droop at either end of the 11-inch drum (see figure B3). This profile was made by means of a Gamma Scientific computer-controlled radiometer equipped with a cosine head receptor with an aperture size of 0.1 in. This is better than the 30-40% droop experienced with the previous source on the earlier scanner table. The spectral distribution of the illumination is shown in figure B4. It is approximately the same as the phosphor blend used in the earlier scanner.

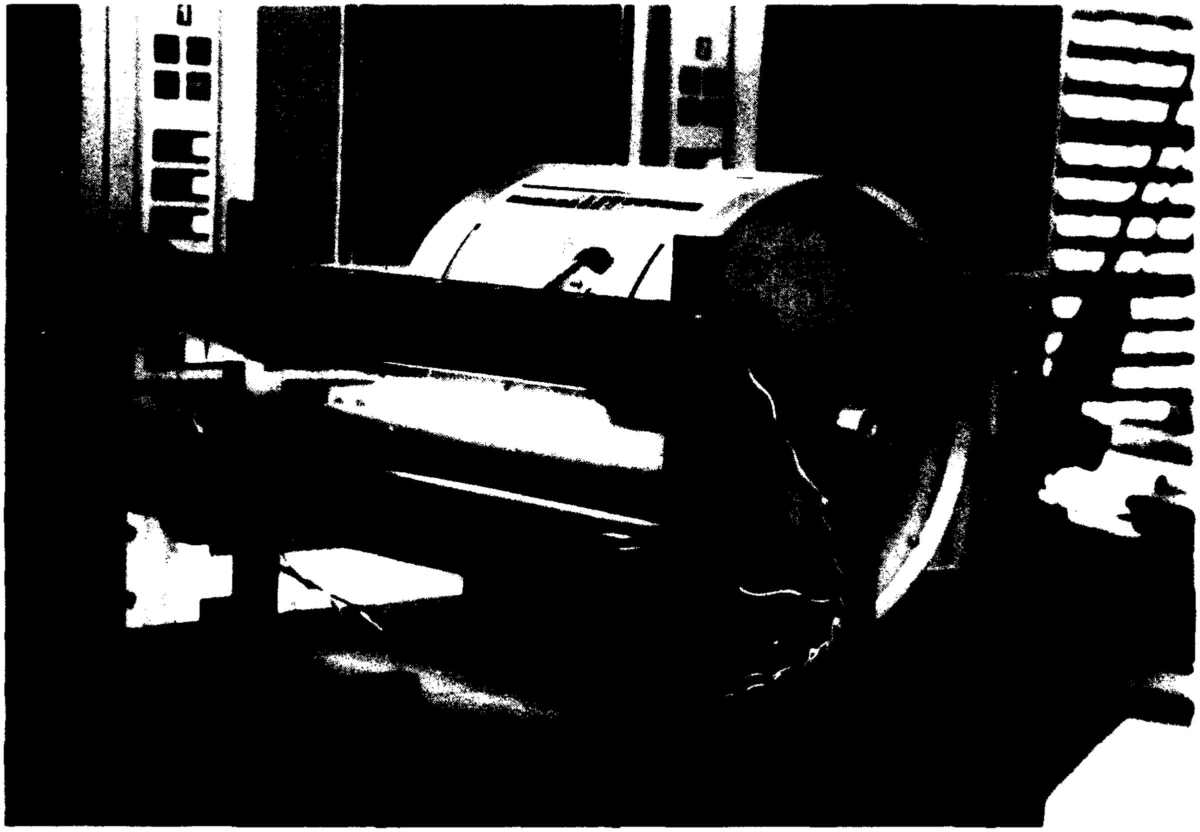


Figure B2. Scanner III illumination source.

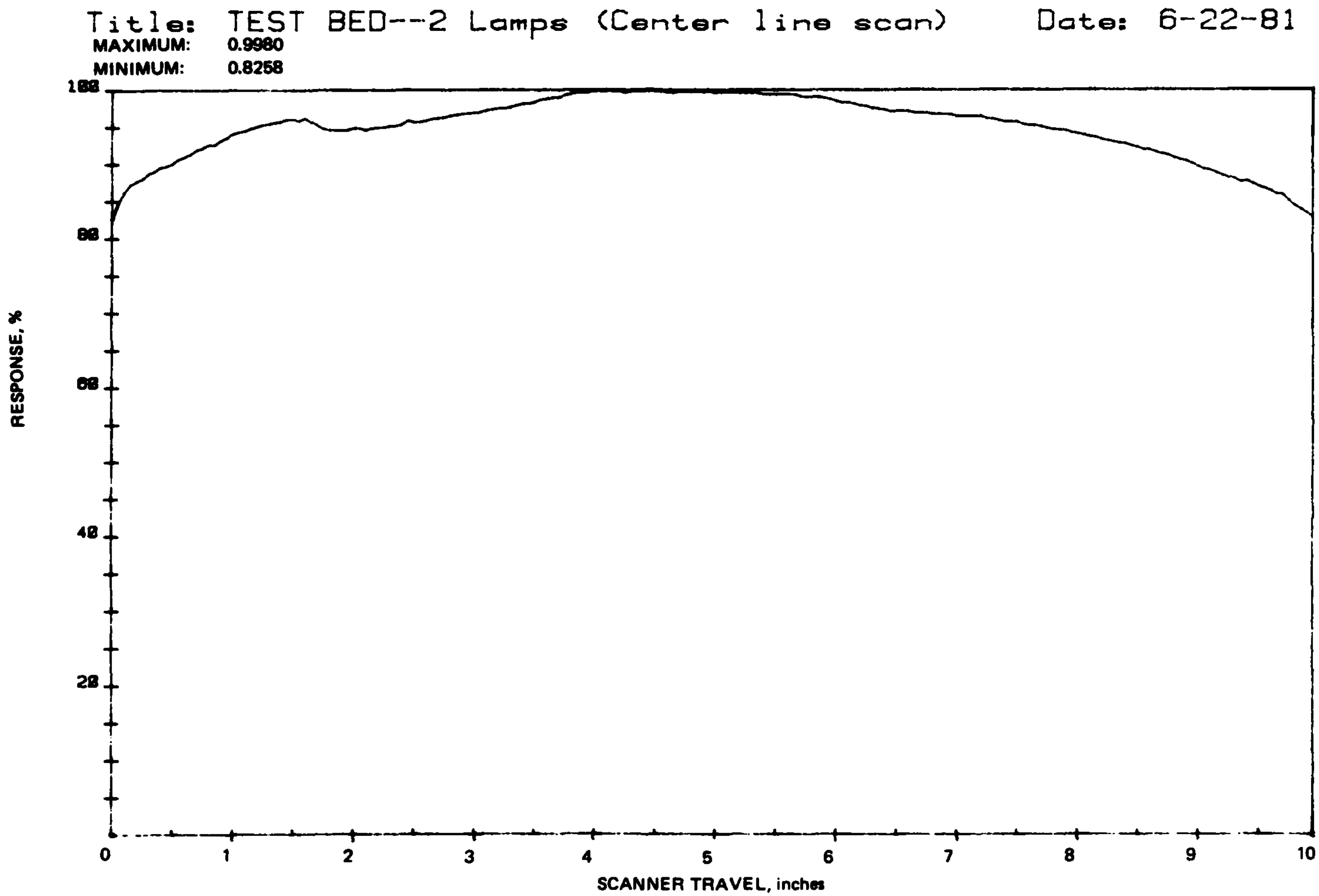


Figure B3. Drum illumination profile.

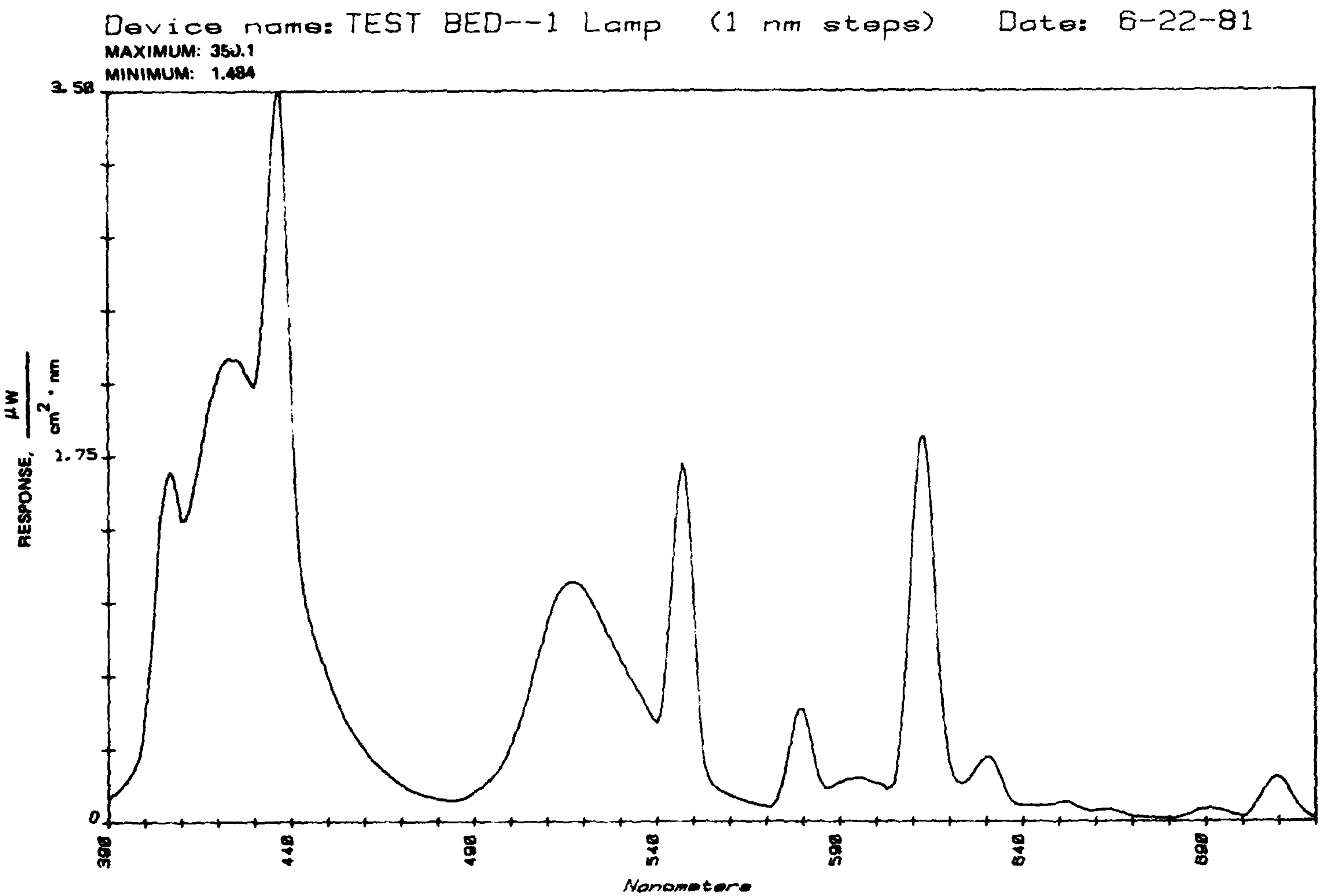


Figure B4. Spectral response of illumination source.

The amplitude of the light actually falling on the drum is about 23.1 milliwatts per square centimeter at the center of the field of view. This is quite a bit below the amount of light needed to cause saturation in the imager at even a 1.5-page-per-second scan rate. The amount of light falling on the imager is found by the equation

$$E_i = \frac{E_d \times R \times T_r}{4\ f^2\ (1 + m)^2} ,$$

where:

E_i = imager illuminance in watts/cm^2

E_d = drum illuminance in watts/cm^2

R document reflectance (about 85% for white paper)

lens transmission (93.3% for the current lens)

f/number of the lens (3.5)

m magnification from document to imager (0.102)

Thus

$$E_i = 0.0134\ E_d$$

$$= 309\ \mu W/cm^2$$

To obtain a value of the actual output voltage level from the CCD 143 imager, the illumination spectrum must be multiplied by the imager spectral response (shown in figure B5). The integral of the resultant curve multiplied by the line integration time yields the output voltage from the imager. The rate at which the imager has been tested to date is about 315 μs/line integration time. This integration time gives an output on the order of 0.35 volts, which is about 17% of the specified 2.0-volt typical saturation output voltage.

This amount of signal is only marginally enough to produce a good bilevel image and is much less than desirable for an 8-bit continuous tone image. It is apparent that more exposure is needed to produce a good quality 8-bit, or even 6-bit, image. This can be obtained by increasing the amount of illumination, decreasing the f/number of the imaging lens, decreasing the scanning rate, or a combination of the above.

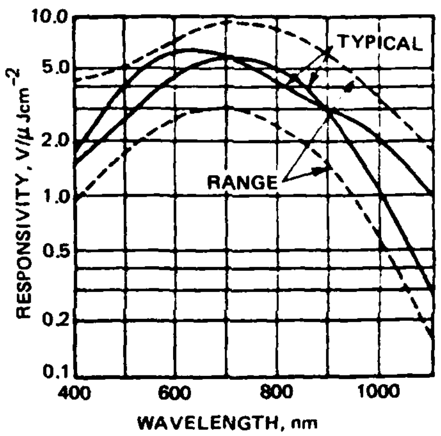


Figure B5. CCD 143 spectral response.

LENSES

The lens currently in use on Scanner III is the Nikon Micro-Nikkor 55 mm f/3.5 flat-field lens. At the time this lens was purchased, it was the optimum choice for wideband use at the resolution of 38.5 lp/mm, its only drawback being its limited speed (f/3.5 maximum aperture). As was shown in the equation above, the amount of illumination available at the image plane of a lens varies inversely with f^2. The aperture of the lens being procured from Alpha Optical by the USPS is f/1.2. This will increase the light available at the image plane by a factor of 6.25. With all other conditions remaining the same on Scanner III this lens would just cause saturation in the CCD 143. This, however, is at a 1.5-page-per-second scan rate.

CCD 143 IMAGER

A number of CCD imaging devices have been tested on ICAS during the course of this program. They include the CCD 110 (a 256-element array), the CCD 121 and CCD 121H (1728 elements), and the CCD 131 (1024 elements). The newest generation of CCD arrays includes the CCD 143, a 2048-pel array with such improvements as enhanced blue response, onboard clock generation, internal sample-and-hold, and lower dark currents. This device has been chosen as a candidate imager for several proposed scanner systems and has been chosen for evaluation and use as a general-purpose scanner at NOSC.

The Scanner Technology Program has been tasked both with investigating the latest developments in the technology and with providing support services, which include scanning various documents for groups such as JPL. To this end, the CCD 143 imager has been designed into a versatile scanner subsystem capable of a variety of scanning operations.

Most of the specifications for the CCD 143 show significant improvement over the earlier devices such as the CCD 131 and the CCD 121H. Some of the more important parameters will be discussed here. The output pel rate of the CCD 143 is guaranteed at 12 MHz, with 20 MHz being a typical maximum achievable rate. Operation on Scanner III has been at 10 MHz thus far with plans for at least testing at 20 MHz. Instead of a guaranteed maximum, the CCD 131 is specified as having a typical rate capability of 24 megapels per second. The CCD 121H is specified at a typical maximum of 10 megapels per second. There has been no significant improvement in the operating frequency of the CCD 143, for the reason that with the inclusion of on-chip clock phase generation, Fairchild could not increase the speed of operation beyond the 20 MHz quoted.

The dynamic range is defined as the ratio of the saturation output voltage to the peak-to-peak output noise of the device in the dark, not taking into account any average dark current component. The typical value of dynamic range specified for the CCD 143 is 1000:1, which is a factor of two better than those of previous imagers. It is planned to make a measurement of the dynamic range of the two CCD 143 devices in the Scanner III test bed as scheduling permits.

The saturation exposure of the CCD 143 is specified at typically 0.67 microjoule/cm^2. This is better than the CCD 131 at 1.0 microjoule/cm^2 but not as good as the CCD 121H at only 0.5 microjoule/cm^2. The operating conditions discussed earlier equate to an exposure value of 0.018 microjoule/cm^2, at which the device is currently being operated.

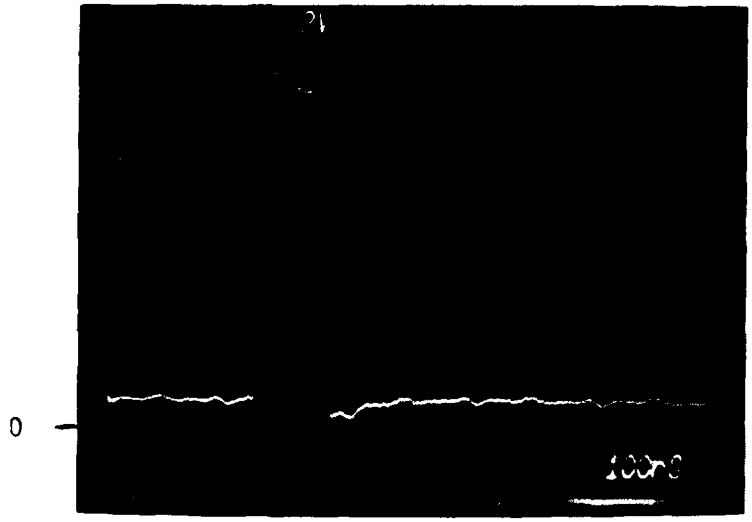
Perhaps the largest improvement in the CCD imagers is in the saturation output voltage, which has increased an order of magnitude from the CCD 121, with 200 millivolts, to the CCD 143, with 2 volts. This helps maintain a higher signal-to-noise ratio in the external analog processing circuitry.

Another feature that significantly reduces the amount of external circuitry around the CCD 143 is the internal clock generation circuitry. This reduces the number of externally supplied clock signals from either four or five down to two, ie a transfer clock and a transport clock. The transfer clock is the once-per-line pulse that transfers the charge from the photosites into the transport registers. The transport clock is used to clock the charge packets out of the imager and operates at a frequency of one-half the pel rate. These clock inputs to the imager present relatively high capacitive loads to the clock drivers: specifically, 300 pf for the transfer clock and 700 pf for the transport clock. The DS0056 clock driver circuit does have enough drive capability to drive the clock lines to the CCD 143. However, only one of the two drivers in each package is used because of the large power dissipation (just over one watt) at a 10-MHz clock frequency. To keep imager noise to a minimum, a separate power supply at +18 volts was provided for the clock drivers. This voltage is regulated to provide independently adjustable high voltage levels for each of the clock signals.

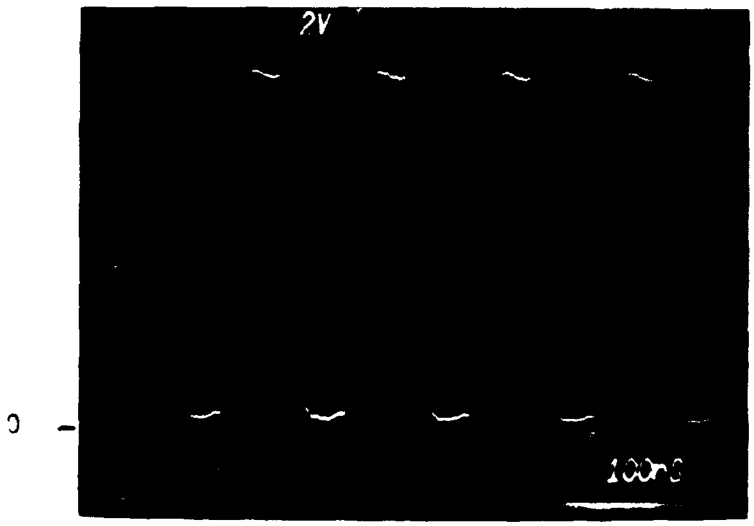
An observation, which is still under investigation, was made of these clock signals. In setting up the imager driver board before the imager was installed, testing was done to assure that the clock drivers were operating properly. Simulated capacitive loads of 300 pf and 700 pf were installed on the board for the transfer clock and the transport clock, respectively. The resulting waveforms are shown in figure B6. When the imager was installed, a significant amount of crosstalk was observed on the transfer clock line (figures B7 and B8). Of particular concern is the fact that the crosstalk on the transfer clock is actually going 300 to 400 millivolts below ground. Any clock transients that go below ground, or below the substrate level of the imager, can cause charge injection. Charge injection results in an increase in the dark signal, which on the CCD 143 has not actually been observed to date. With the CCD 121 and CCD 121H imagers, this same problem existed and the substrate had to be biased a few hundred millivolts below ground.

The video outputs from the imager are buffered through recommended emitter followers, then ac-coupled into LH0033 buffer amplifiers to remove the 8-volt dc signal component. The video outputs at the driver board are shown in figure B9, with the two channels at very close to saturation exposure. The actual saturation output voltage as measured at the outputs of the imager is about 1.75 volts. For these photos, the imager is looking at the 10-line-per-inch bar pattern on the IEEE Facsimile Test Chart. The upper "baseline" of each trace is the clock feedthrough signal. About 300 mV down is the black- level signal and about 1.3 volts more negative is the white-level signal. The profile of the most negative portion of the trace is representative of the overall illumination profile across the drum.

Figure B10 shows the timing relationship between the two output channels, A and B, of the imager. It can be seen that the two channels are out of phase, allowing a straightforward multiplexing scheme for processing the image data.

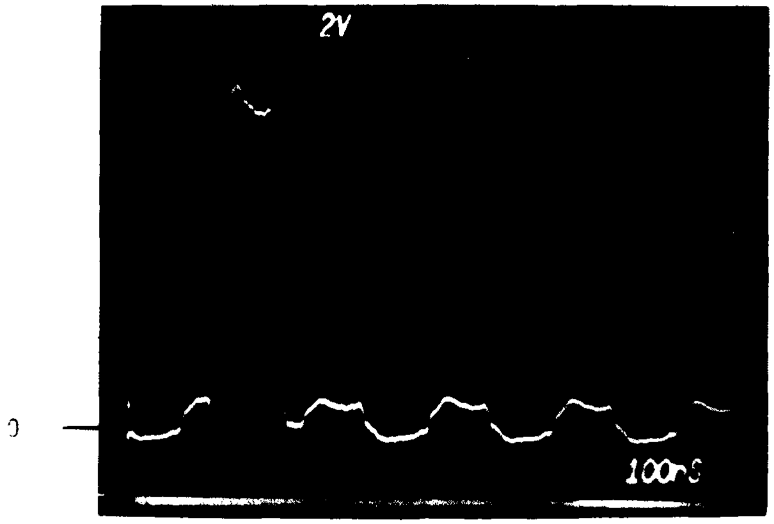


a. Transfer clock.

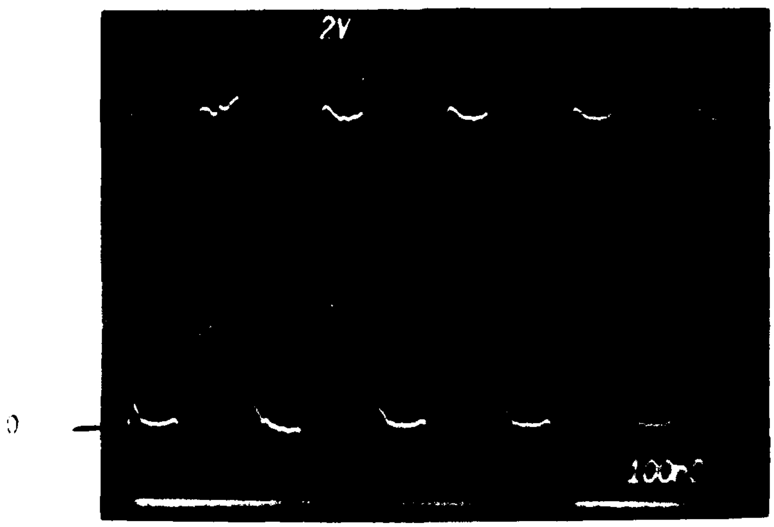


b. Transport clock.

Figure B6. Clock signals with simulated loads.



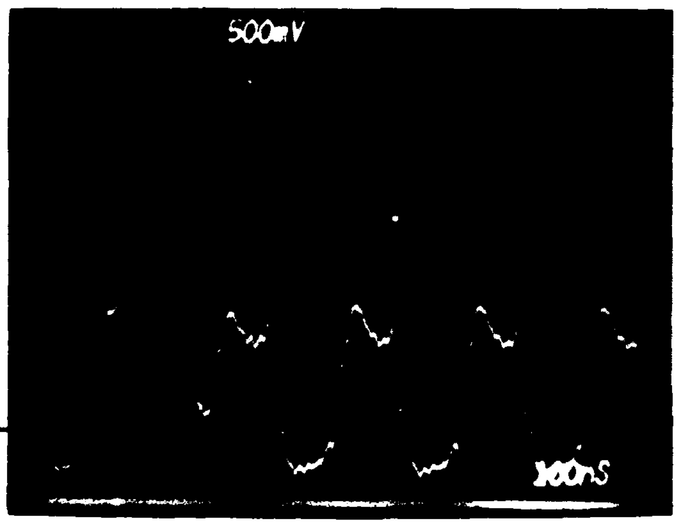
a. Transfer clock.



b. Transport clock.

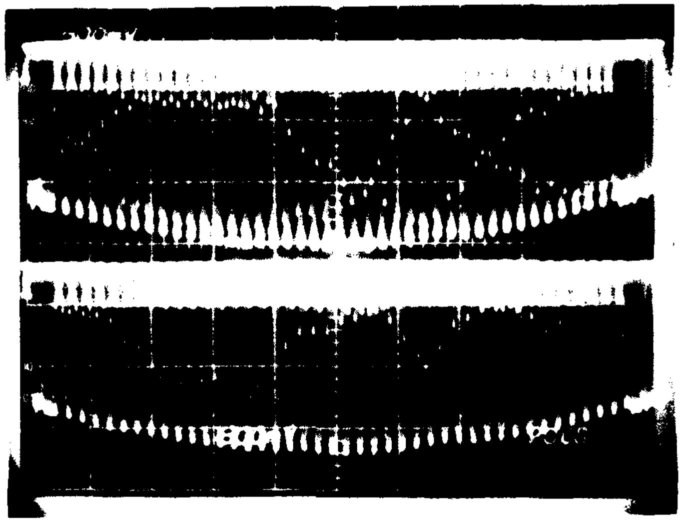
Figure B7. Clock signals with imager installed.

a. With simulated load.

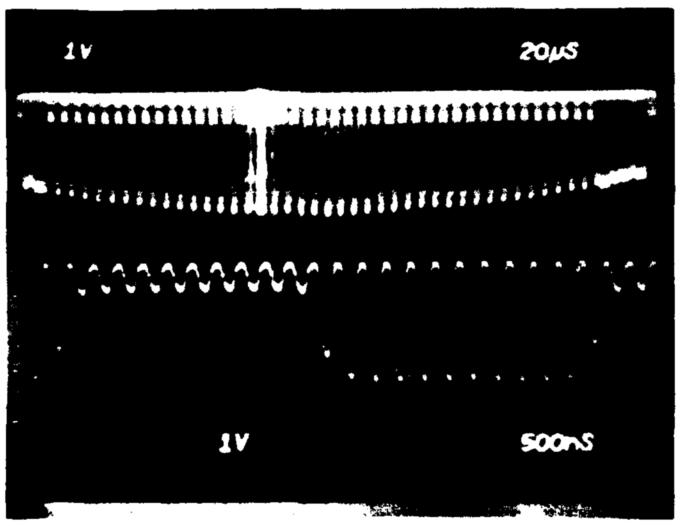


b. With imager installed.

Figure B8. Comparison of transfer clock signals at increased vertical sensitivity.



a. Top trace: channel A; bottom trace: channel B.



b. Channel B with intensified portion shown expanded in bottom trace.

Figure B9. CCD 143 outputs at driver board.

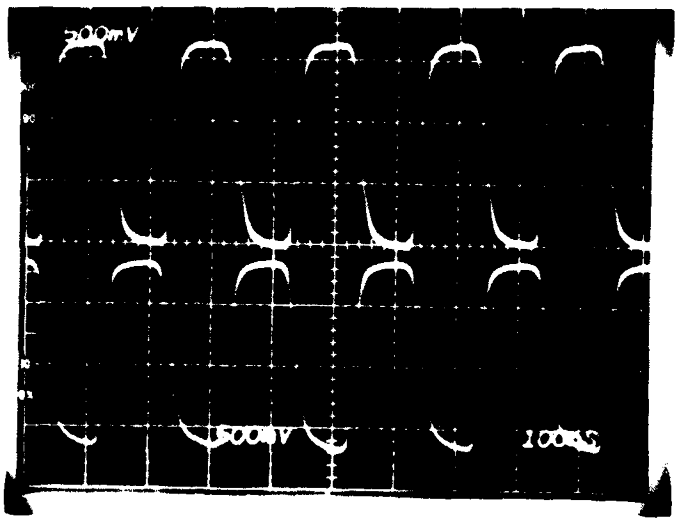


Figure B10. CCD 143 driver board outputs at expanded time scale.
Top trace: channel A; bottom trace: channel B.

Because it was desired to control the scanner from the ICAS operator's console, an IEEE-488 (GPIB) interface was incorporated into the digital control logic of the CCD 143 scanner card set. This allows commands and setup parameters to be transferred to the scanner and digitized data to be transferred to the system controller (the Tektronix 4054).

The CCD 143 control board consists primarily of the GPIB interface and a number of registers and counters, which directly control virtually all of the scanning parameters. Figure B11 shows a block diagram of the CCD 143 control. Each setup and control register is assigned a unique address. To establish a value in a register it is necessary only to address the interface to receive data, then to transfer pairs of bytes over the GPIB. Each byte pair consists of a register address followed by the contents of that register.

There are seven CCD 143 registers: control register, vertical resolution, lines delayed, lines captured, integration time, pels delayed, and pels captured. In addition, the command to initiate a capture operation is treated as a register with its own address.

The control register consists of six bits used as switches for various scanner operations. Normal/continuous capture select determines whether the "data available" signal will be true always (continuous) or for only one capture operation after a drum sync (normal). Line delay enable determines whether a capture will begin immediately after data available (DAV) goes true (normal) or after a number of lines specified by the "lines delayed" register (enabled). Drum sync enable is used in conjunction with normal/continuous select to determine whether a capture operation starts at drum sync or immediately upon receipt of a capture command. The integrate/shift control determines whether integration and shifting are performed simultaneously or sequentially. Encoder clock enable determines whether the individual lines are captured on the basis of the linear distance travelled by the drum surface (enabled) or by the integration time (disabled). Bit precision select allows either 6-bit or 8-bit pels to be captured.

The other registers, ie vertical resolution, integration time, lines captured and pels per line captured, are generally self-explanatory. Lines delayed is the number of lines to be delayed after the capture sequence begins and before lines are actually captured. This is subject to enabling of the delay. Pels delayed is simply the number of pels on a line that are skipped before actually capturing pels.

ANALOG PROCESSING

The analog processing circuitry is designed to amplify the two-channel video output signals from the CCD 143, multiplex them, and perform the A/D conversion to either 6-bit or 8-bit pel information. Two fundamental approaches were considered for this processing task. Two separate output channels from the imager allow individual adjustment of gain and level in order to balance the two channels. From this point, one approach is

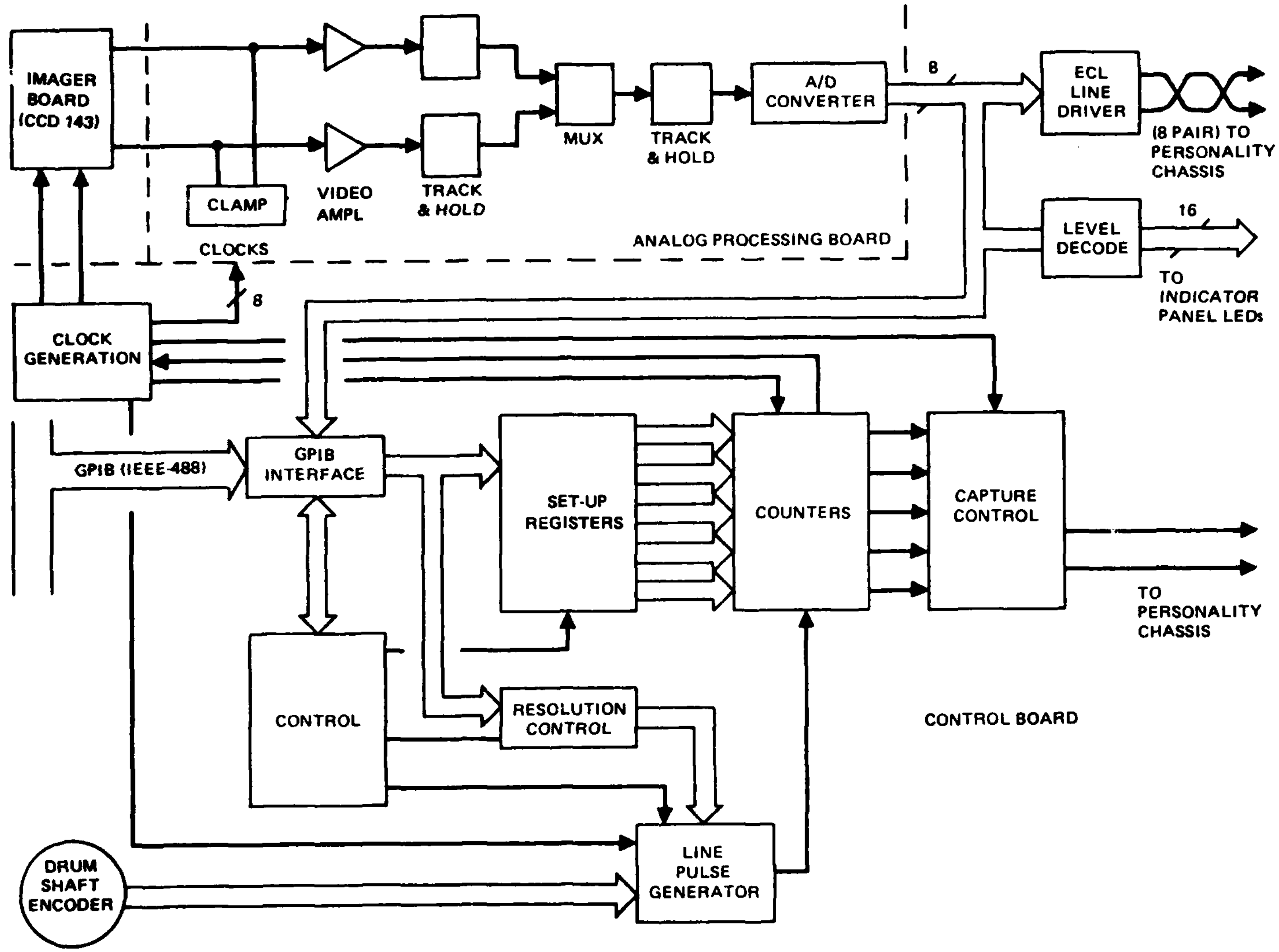


Figure B11. CCD 143 control.

to use two A/D converters and combine the digital outputs when storing the image data in memory. A second approach is to multiplex the two analog signals and then use only one A/D converter to perform the conversion. The decision was made to take the latter approach because complete characterization of the four TRW converters had not yet been completed. It was felt that any odd-even problems that might exist due to differing converter characteristics would therefore be avoided in acquiring images. In addition, the analog circuitry has been designed in a modular fashion, which will allow an easy transition to the former approach should that action be deemed desirable.

A block diagram of the analog circuitry is shown in figure B12. There are two processing channels, each containing an amplifier with a dc clamp, individual gain and level controls, and a track-and-hold (T/H) amplifier. Following the T/H amplifier, the two channels are multiplexed together and input to a third T/H amplifier to remove switching transients before being input to the A/D converter. The dotted lines in figure B12 show the physical division of the circuitry into three sections. Each section is built on a 4-inch by 6-inch card which is then mounted on an 8-inch by 15-inch board that plugs into the Scanner III electronics card cage. Figure B13 is a photo of the completed board. The three sections shown in figure B13 correspond left-to-right to the block diagram of figure B12.

The analog input for channel A is buffered and ac-coupled into a dc clamp circuit. The dc clamp is made up of two D-MOS n-channel FETs, which clamp the video signal to ground after each pel is output from the imager. Figure B14 shows the timing relationship between the dc clamp drive signal (first and third traces) and the channel A video signal (second and fourth traces). The upper two traces show an entire image line, while the lower two traces show an expanded version (faster time scale) of the intensified portion of the upper traces. The active clamp time is during the high state shown on the trace, which corresponds to the output transistor reset time in the imager. The valid pel output time is during the negative portion of the video waveform. In all of the photographs shown of analog video signals, the brighter the image, the more negative the signal.

Following the dc clamp, the analog video signal is amplified by an Optical Electronics, Inc 9909 operational amplifier, which is set up with a fixed gain of 15 dB in a noninverting mode. The level of the signal is adjusted so that the output dark level is at +1.0 volt and the white level swings negative to -1.0 volt. Gain balancing of the two channels is provided for by two potentiometers on the output of the amplifiers. The bandwidth of the amplifiers in this configuration is over 40 MHz at the 3 dB point.

On the inputs to the final buffer amplifiers, there is a limiting circuit comprised of four diodes in series. This circuit is used to limit the reset clock feedthrough which is present on the video signal. When the imager is operating at about 17% of saturation, the reset clock feedthrough portion of the signal has about the same amplitude as the dark-to-light transition. After the amplification, there is enough signal to overdrive the T/H amplifier.

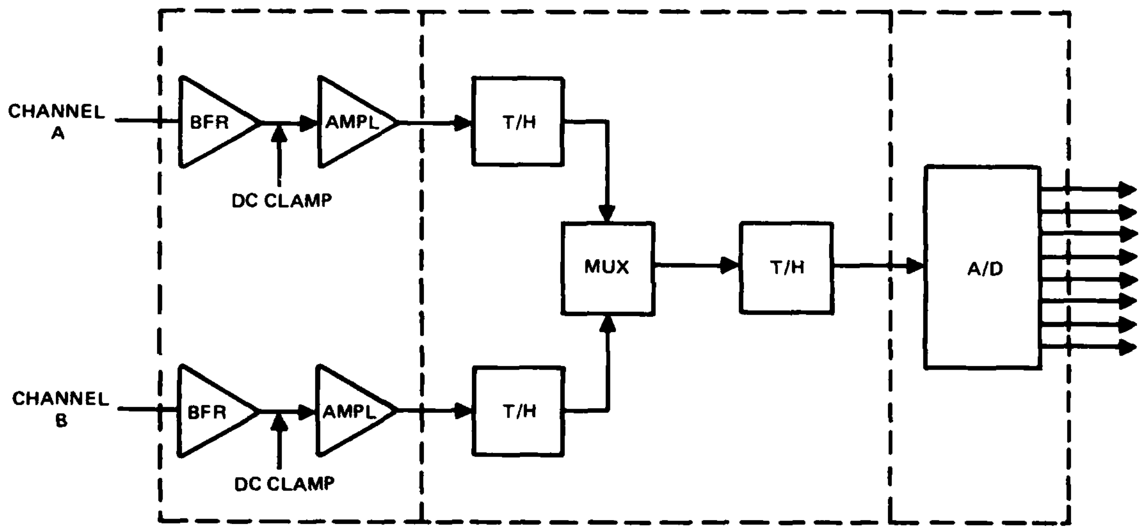


Figure B12. CCD 143 analog processing block diagram.

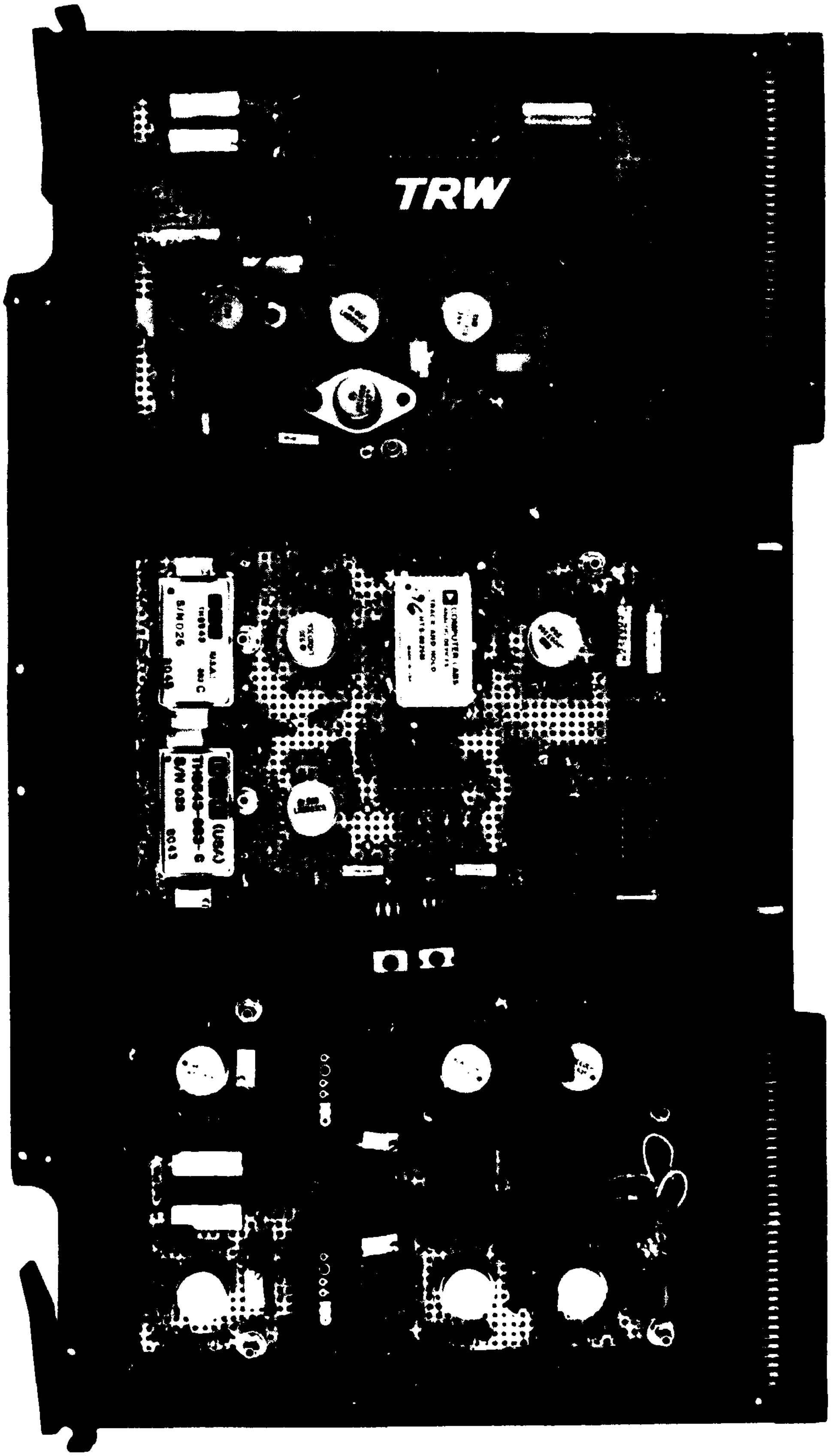


Figure B13. CCD 143 analog processing board.

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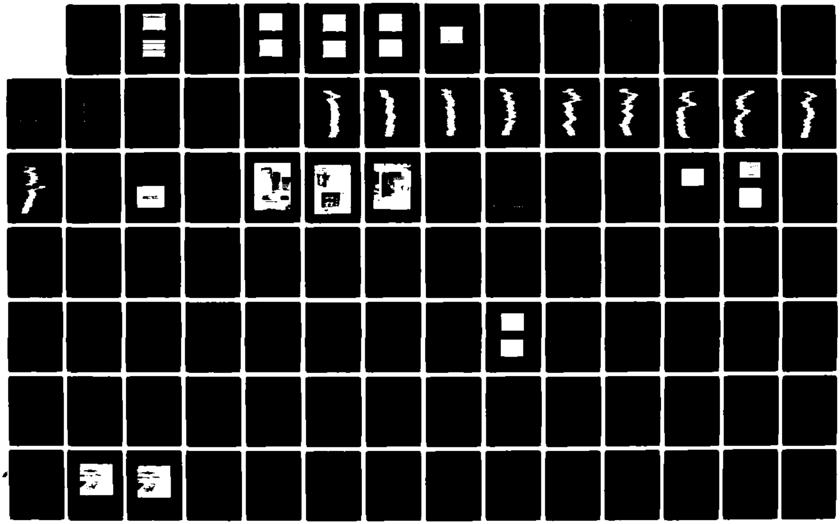

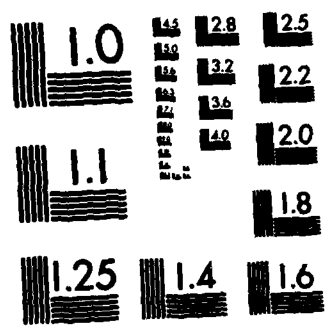

MICROCOPY RESOLUTION TEST CHART
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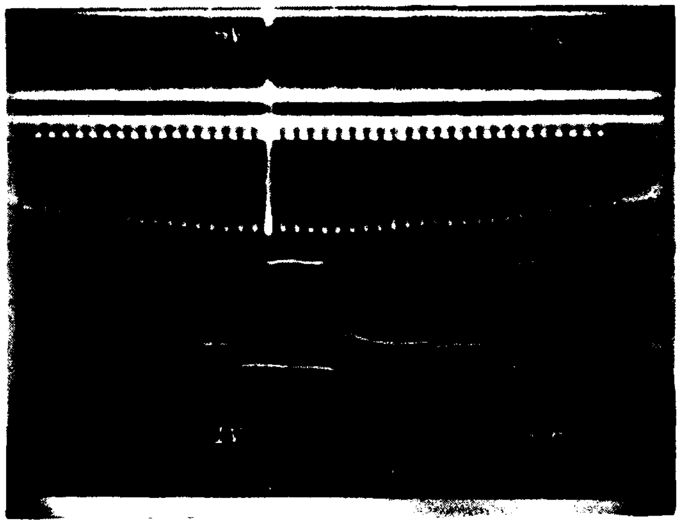


Figure B14. Timing of dc clamp and video output for channel A.

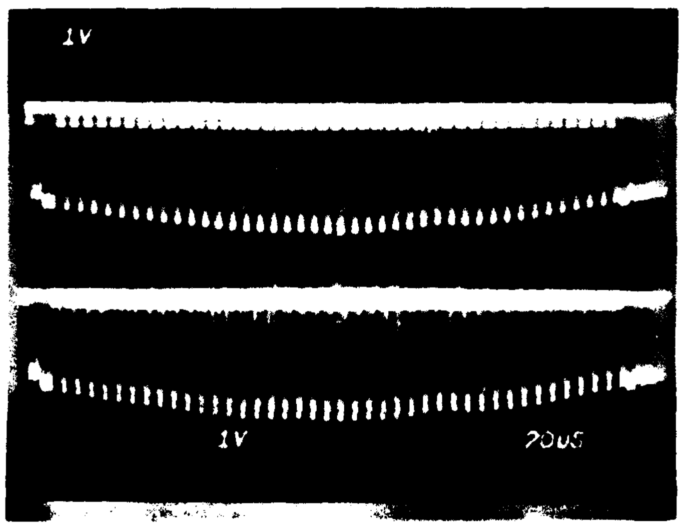


Figure B15. Video amplifier outputs. Top: channel A; bottom: channel B.

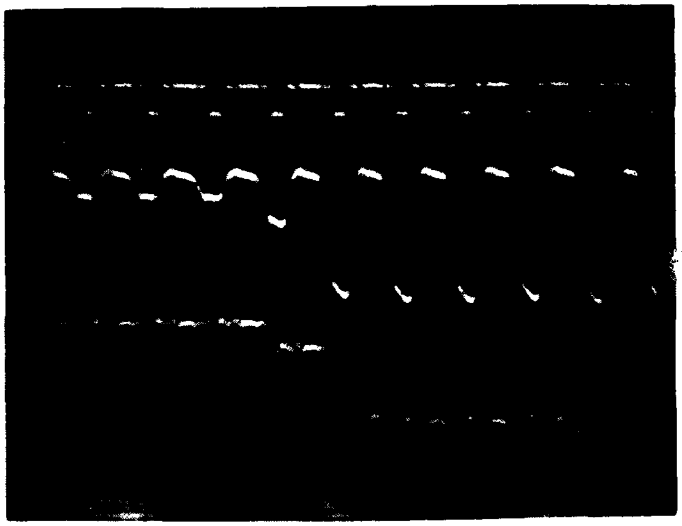
The diode circuit limits the clock feedthrough to 150 mV above the dark pel level of +1.0 volt. The final output of the amplifier section is shown in figure B15.

The two analog signals output from the video amplifier section are input to the second section of the analog processing circuitry (middle circuit board) via RG/174 coaxial cables. Here, each signal is input to a T/H amplifier (DDC-8534), which has a small-signal bandwidth of 80 MHz and a maximum rate of 40 megasamples per second. This T/H amplifier also has a 1-volt built-in offset so that for a +/- 1-volt input there is a zero to -2.0-volt output voltage range. This unit was designed specifically for use with the TRW 8-bit A/D converter. Figure B16 illustrates the operation of the T/H amplifier. The top trace is the hold command. When this signal is in the low state, the output (bottom trace) follows the input (middle trace). When the hold command goes high, the output is held at the current voltage level.

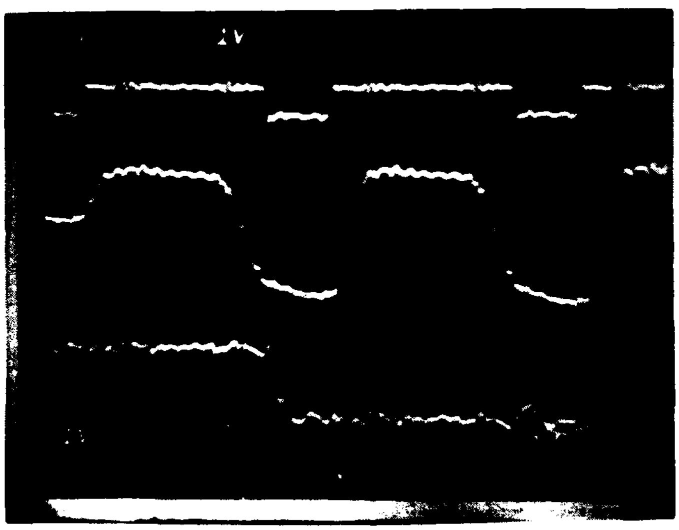
The next step in the process is the multiplexing of the two channels of video into a single pel stream. This is accomplished by means of two FET switches. The operation of this circuit is illustrated in figure B17. The top trace is the multiplexer control signal. The signal selects channel A when high and channel B when low. The second trace shows the channel A T/H output. The third trace is of channel B. The bottom trace is the multiplexer output. There is some switching noise on the multiplexed signal. To remove this noise, a third T/H amplifier, the Analog Devices HTS-0025, is used. This T/H has a +/- 2-volt input range with no offset, a 30-MHz bandwidth, and a 30-MHz sample rate. Figure B18 shows the operation and resultant output from the analog processing circuitry. The top trace is the multiplexer control, the second trace is the hold command, the third trace is the multiplexer output, and the bottom trace is the final output.

In figures B16 through B18, it should be noted that all the signals except the T/H output (bottom trace in figure B18) were acquired with conventional scope probes. With these probes, there is some noise pickup due to the length of the ground leads and any special input leads used. The T/H output was coupled directly into a 50-ohm plug-in via coaxial cable and thus shows very little noise as compared to any of the other traces.

The final section of the analog processing board contains the TRW TDC 1007J 8-bit A/D converter. This converter has a maximum guaranteed conversion rate of 20 MHz. The input voltage range is zero to -2.0 volts. The analog input signal is double-buffered, with one buffer driving the A/D and the other buffer providing a monitor output for setup and balancing operations. Figure B19 shows the input timing waveforms for the converter. The top trace is the convert command, the rising edge of which actually initiates the conversion. Internal to the A/D is a two-stage pipeline delay. When the convert command is issued, the second previous conversion result is available on the outputs. The detailed characteristics of the A/D converter will be presented in a later section.

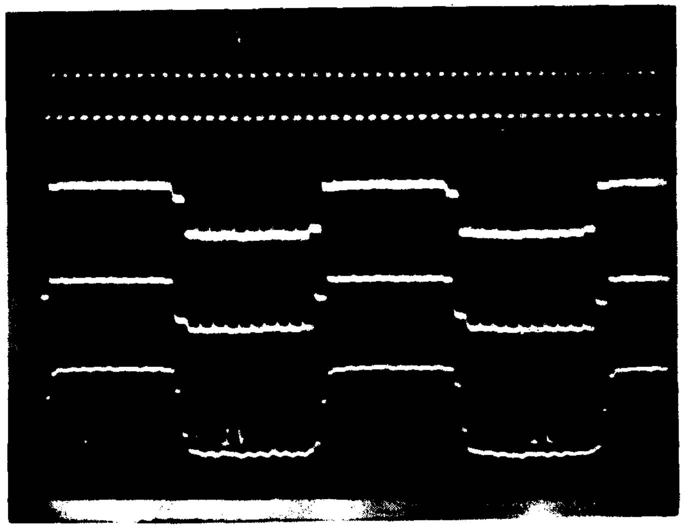


a. Time scale – 200 ns per division.

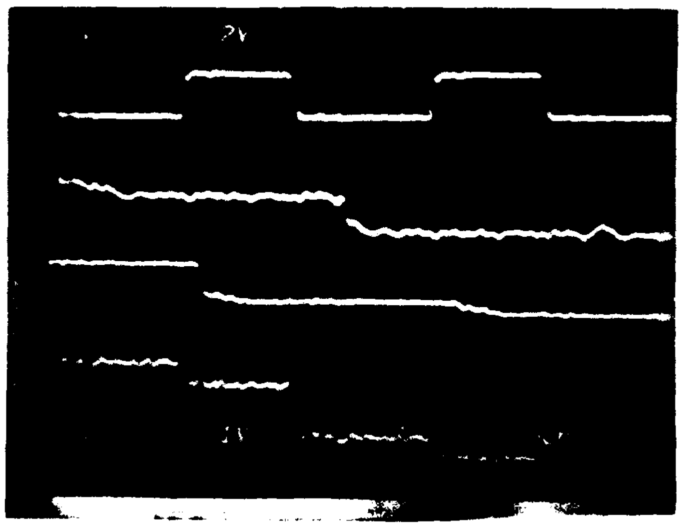


b. Time scale – 50 ns per division.

Figure B16. Track-and-hold amplifier waveforms.

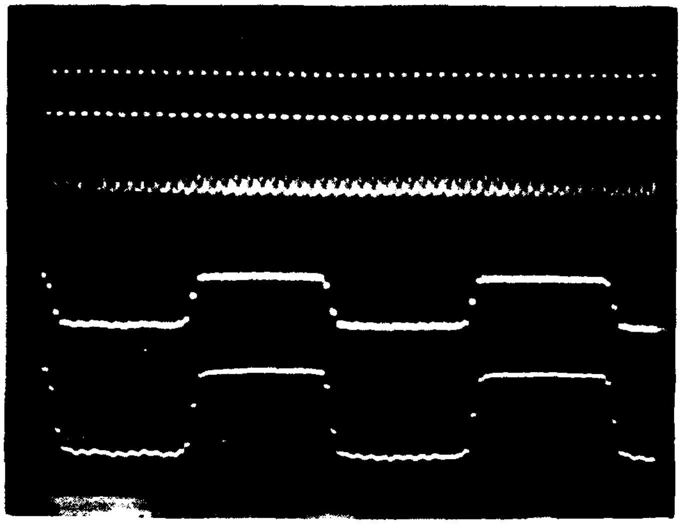


a. Time scale – 1 μs per division.

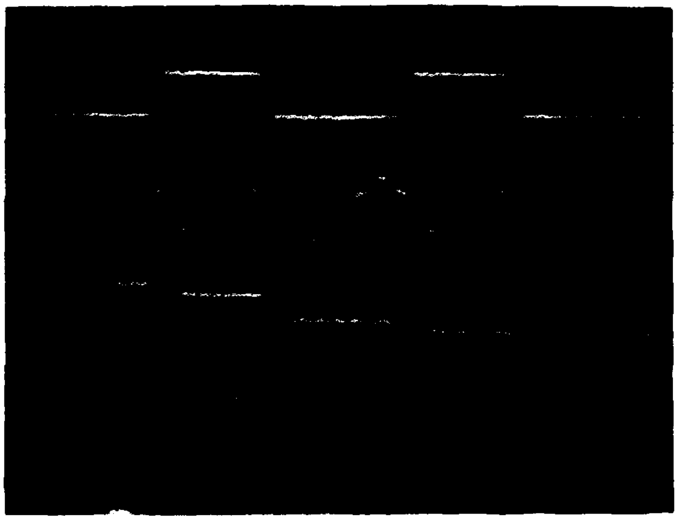


b. Time scale – 50 ns per division.

Figure B17. Analog multiplexer showing control signal, two analog channels, and multiplexed output.



a. Time scale – 1 μs per division.



b. Time scale – 50 ns per division.

Figure B18. Multiplexed video track-and-hold amplifier timing.

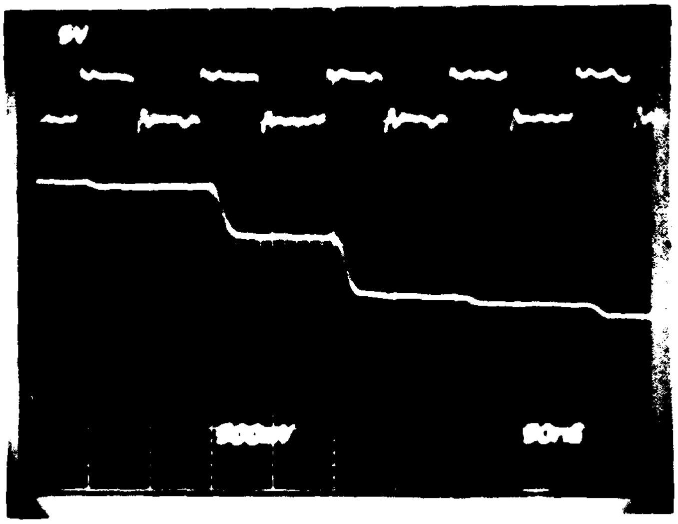


Figure B19. A/D converter timing. Top trace: convert command; bottom trace: analog input.

PROCESSING FOR 6-BIT AND 8-BIT RESOLUTION

With the current effort aimed at acquisition of images at 8-bit resolution, software is being revised to allow the processing of pels at either 6-bit or 8-bit resolution. Both resolutions must be provided for to insure the versatility to accommodate any required format or processing function.

The primary impact upon the software results from the difference in memory organization between the two resolutions. At six bits, a memory word consists of eight pels. At eight bits, the same word consists of only six pels. The software revisions entail the locating of individual pels for processing based upon a few parameters that are set once when a format modification is made.

Currently, the only way to display at 8-bit resolution those images captured at eight bits is to transfer a portion (512 x 512) of an image to the COMTAL image processing system. For this reason, the COMTAL control software was the first to be modified to allow access to either 6-bit or 8-bit data.

The other programs in process or intended for conversion are output to the color film recorder, illumination correction, filtering, function tables, and statistical analysis.

HIC AND HEE

The hardware illumination corrector (HIC) and the hardware edge enhancer (HEE) have been delivered and accepted by NOSC. The design of this equipment contains many data paths in the hardware for self-test routines generated by the GNAT 10 microcomputer supplied with the HIC and HEE as a system controller. Originally, a major problem was encountered relative to the wiring of power and ground to all the integrated circuits in both systems, causing serious noise problems. This and other problems, eg timing and data sensitivity, were rectified after significant effort by both contractor and NOSC personnel. (Included as annex A to this appendix is an investigation into the problems encountered when implementing the latest technology TTL logic circuits in very-high-speed applications.)

Extensive software has been provided for the test and debug as well as the on-line control of the HIC and the HEE. In keeping with the "user friendly" approach to system programming, menus and self-explanatory prompting are provided for ease of operation. Two basic commands were provided for debugging and one provides for on-line control.

The "HIC" command allows complete control of the HIC and the HEE, including loading of the calibration RAM (CRAM) and the function RAM (FRAM), activation and deactivation of the HIC and HEE functions (independently of each other), and setting of the HEE gain constant.

In normal operation, the CRAM is loaded with an illumination curve and the FRAM is loaded with a multiplication table. The HIC command provides the capability of adding a transfer function to be incorporated directly into the multiplication table. This allows transforms, such as thresholding at any level, to be built into the correction process.

For testing purposes, the CRAM and FRAM can be loaded with any known pattern to allow checks for a known input and the expected output vs the actual output.

Figures B20 and B21 are examples of the performance capability of the HEE. Figure B20 shows a portion of an image line through the 10-line-per-inch square wave on the IEEE Facsimile Test Chart. The upper line is unenhanced and the lower line is enhanced with a gain of one. Because these two lines were acquired on separate passes, it cannot be guaranteed that line 2 is an exact enhancement of line 1 but the general characteristic is exactly what would be expected. Figure B21 shows the results of an identical operation on a line of alphabetic characters set in pica type.

Observation of the image waveforms reveals that the algorithm was, in fact, performed correctly, ie low-intensity pels next to high-intensity pels are lowered further and high-intensity pels next to low-intensity pels are increased in intensity. It can also be seen, however, that there is an alignment problem between channels in the scanner analog circuitry. This

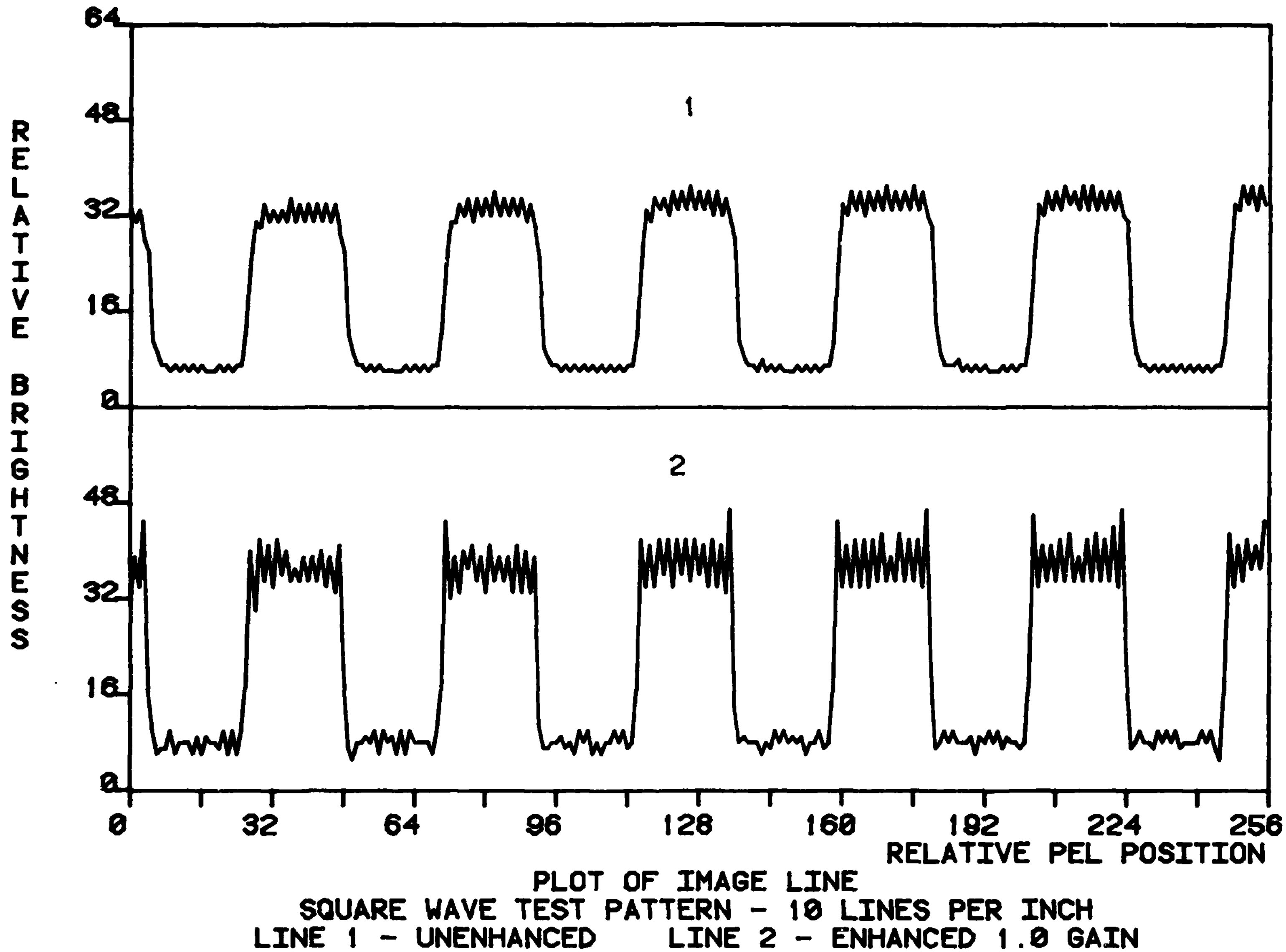


Figure B20. Image lines--square wave test pattern, unenhanced vs enhanced with gain = 1.

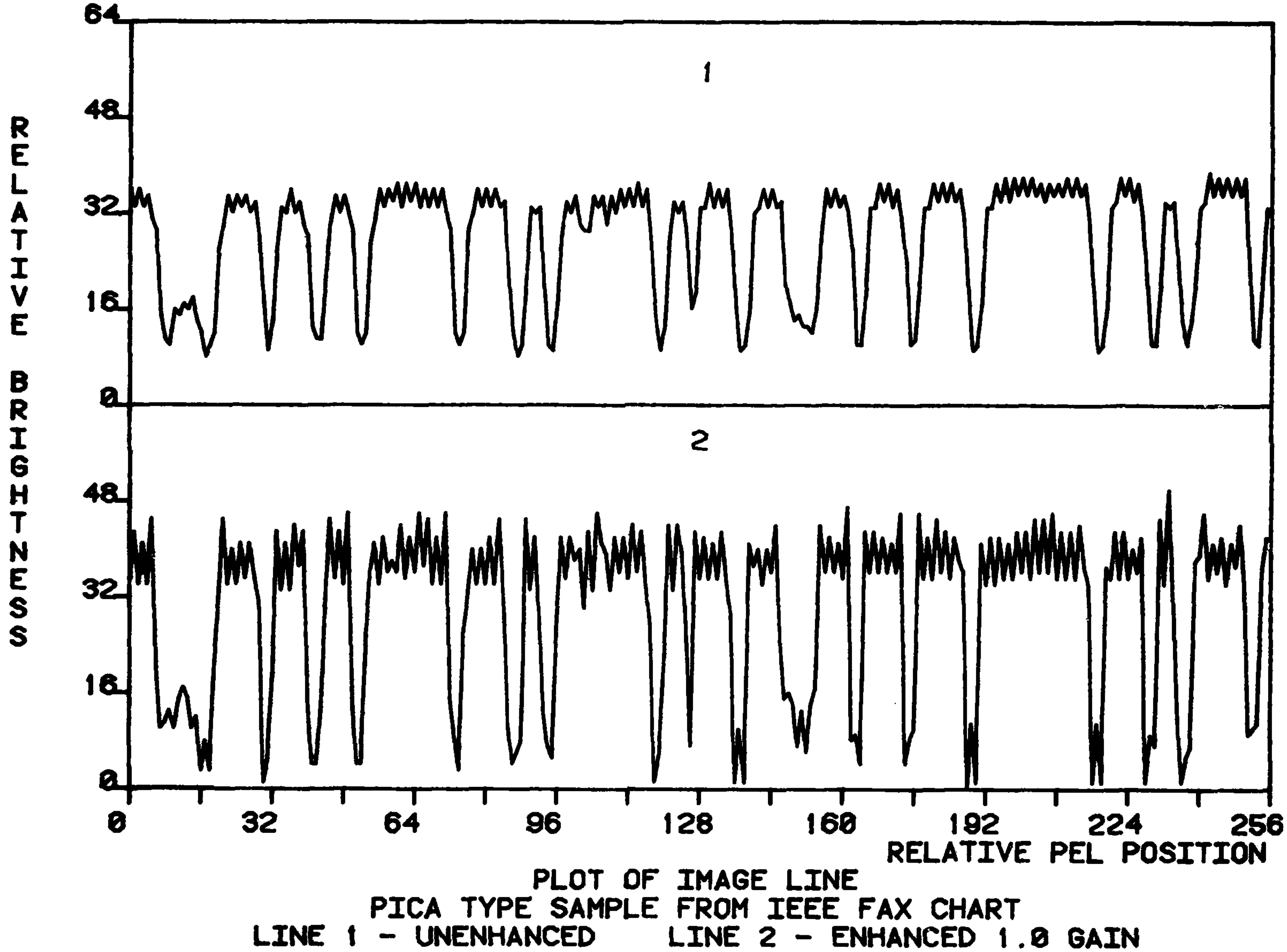


Figure B21. Image lines—pica type sample from IEEE FAX chart, unenhanced vs enhanced with gain = 1.

misalignment is most apparent at the higher intensity levels of both the square wave and the line of type. As a result of the misalignment, and with a high-gain constant used, the enhancement process tends to accentuate the disparity between channels.

An additional problem uncovered results from the enhancement of noise impulses unrelated to the consistent misalignment noise. An individual noise impulse in a uniform background will not be altered, but it can cause all pels immediately surrounding it to be altered in the direction opposite from the impulse. This error results from the conditions which determine whether or not a pel will be enhanced (see page 84, reference B1, below).

To retain the beneficial effects of enhancement and avoid the problems mentioned, an attempt was made to eliminate the noise from the image prior to performing the enhancement. In a software simulation of the algorithm, the selective filter method (described in reference B2, page B-35) was applied to the data prior to the enhancement. Indications from past experience were that the filter would decrease the fluctuations due to the odd-even problem of the imager. The basic stop band filter of a one-pel run and a delta of one brightness level was increased to include either of the following conditions:

One pel run and delta up to two brightness levels

One pel run and delta of one brightness level immediately followed by a delta of two levels in the opposite direction

The results of this operation (labeled filter A) are shown in figure B23. (Figure B22 shows the actual enhancement of the square wave from figure B20.) It is easily seen that the variation at the lower intensities is decreased considerably. The variation at the higher intensities, which is on the order of three or four levels, remains virtually unchanged.

As an attempt to decrease this variation, another filter (filter B) was used, this time with the delta range changed to four levels rather than two. The result, shown in figure B24, indicates that a great deal of the variation can be removed by using this type of filter. The filter must be applied very carefully, however, as can be seen in figure B24. If the image is to be thresholded after enhancement, a great deal of the white areas would end up as black areas with a white edge, depending upon the threshold level chosen. It does appear, however, that there is promise in the use of a filter of this type in sequence between the illumination correction and the edge enhancement procedures.

B1. NOSC Technical Report NELC TR 1965, First Annual Report, Advanced Scanner Technology, October 1975.

B2. NOSC TR 358, Fourth Annual Report, Advanced Scanner Technology, October 1978.

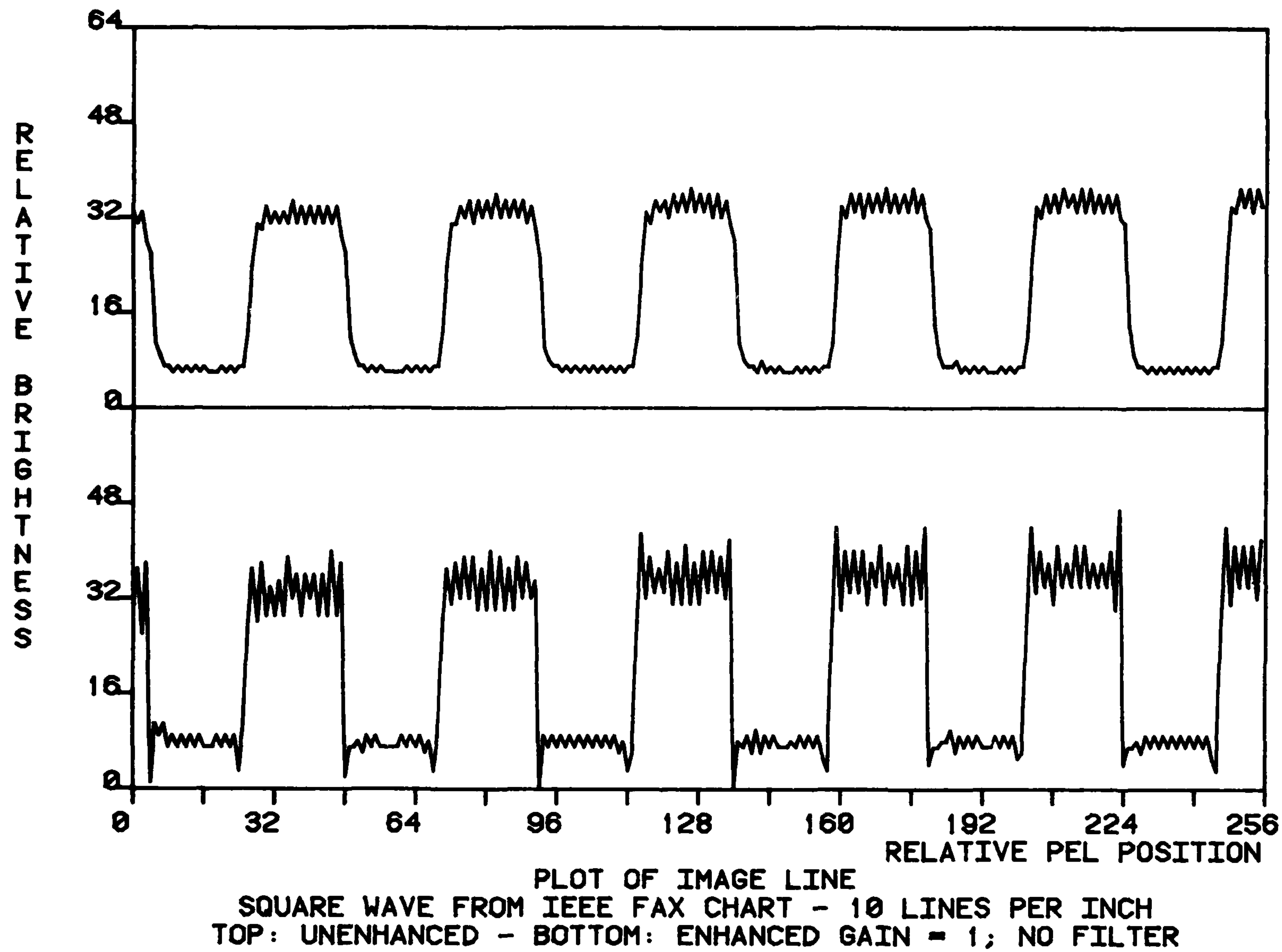


Figure B22. Image lines–square-wave test pattern with no filter, unenhanced vs enhanced with gain = 1.

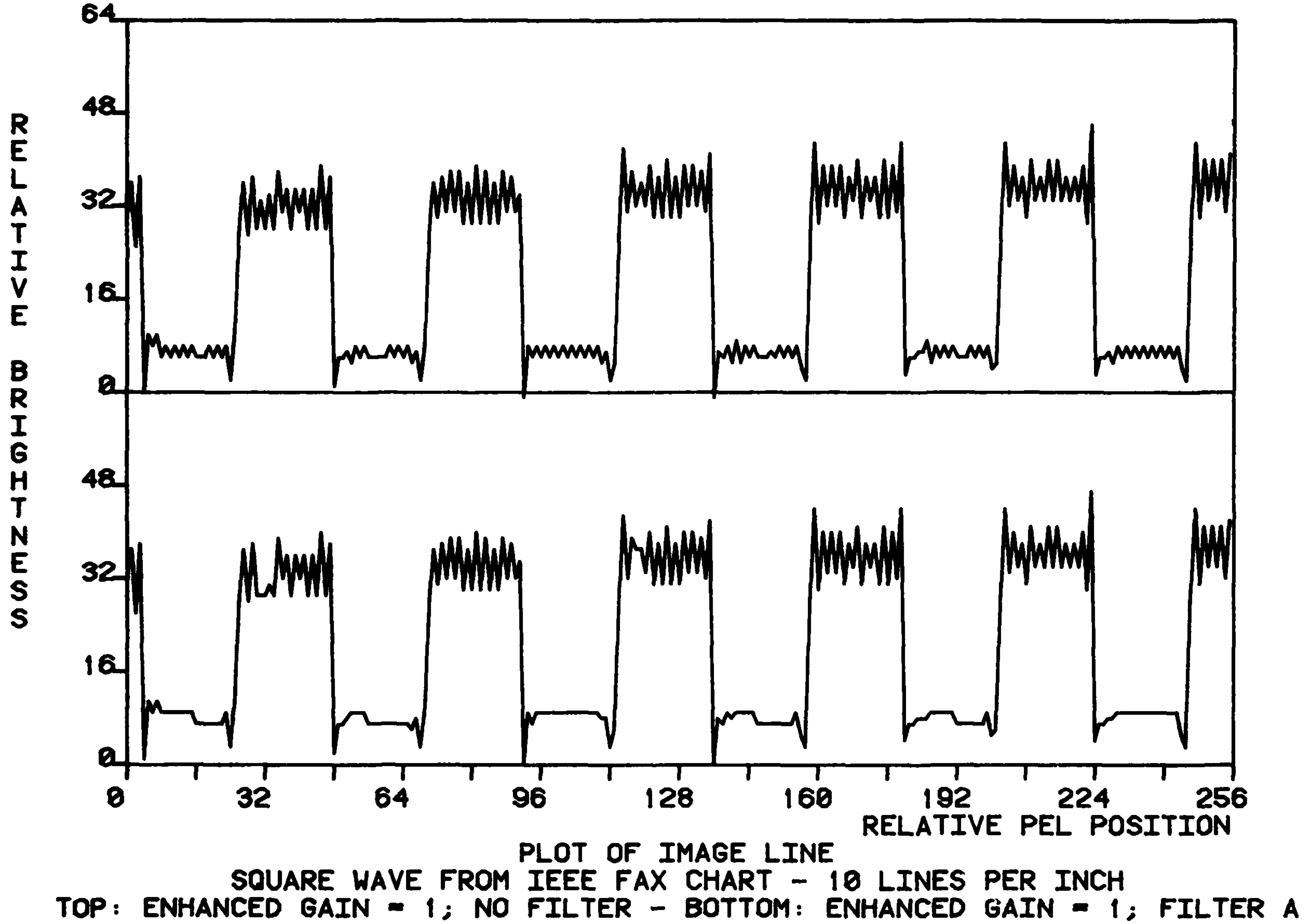


Figure B23. Image lines - square-wave test pattern enhanced with gain = 1, no filter vs filter A.

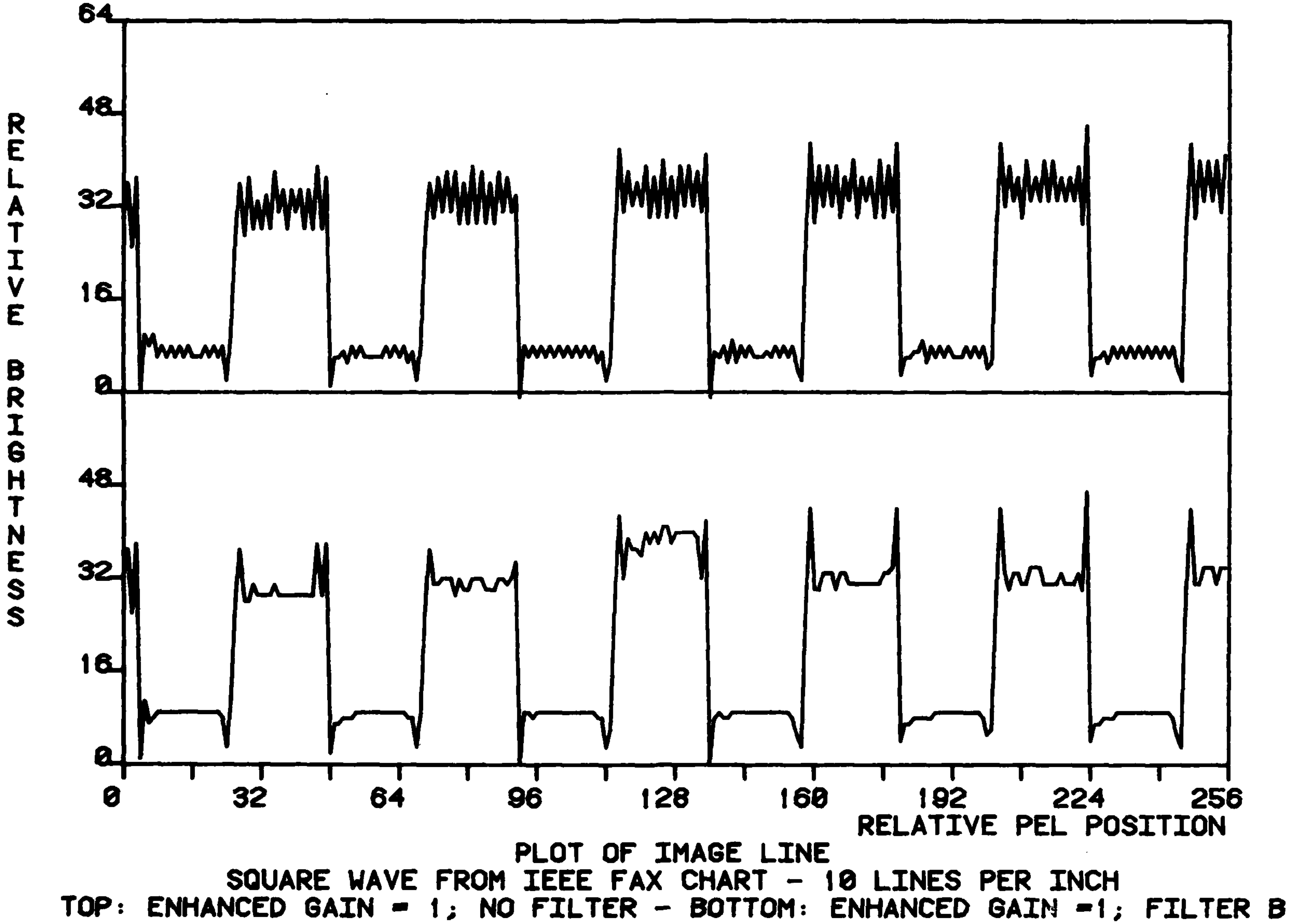


Figure B24. Image lines—square-wave test pattern enhanced with gain = 1, no filter vs filter B.

A/D CONVERTER TESTING

Prior to the implementation of Scanner III, A/D converters were self-contained units that were "plugged into" the data path. The philosophy behind Scanner III is to have a set of analog and digital cards for each imager used and to have the A/D converter(s) mounted directly on the analog card. The digital control of the scanner is accomplished via the IEEE-488 interface bus (GPIB). Because of the proximity of these two sets of circuitry, it was decided to allow the interface to read single pels and place them on the bus for analysis by the 4054. In combination with a waveform generator and a digital voltmeter (DVM), also controlled via the GPIB, the A/D can be tested for its output at a known input voltage level.

The equipment and interconnection for testing is shown in figure B25. The 4054 acts as controller and data collector for the operation. The waveform generator provides an analog input to the scanner, and the DVM provides an accurate reading of the analog voltage actually input to the converter. The testing procedure is outlined below.

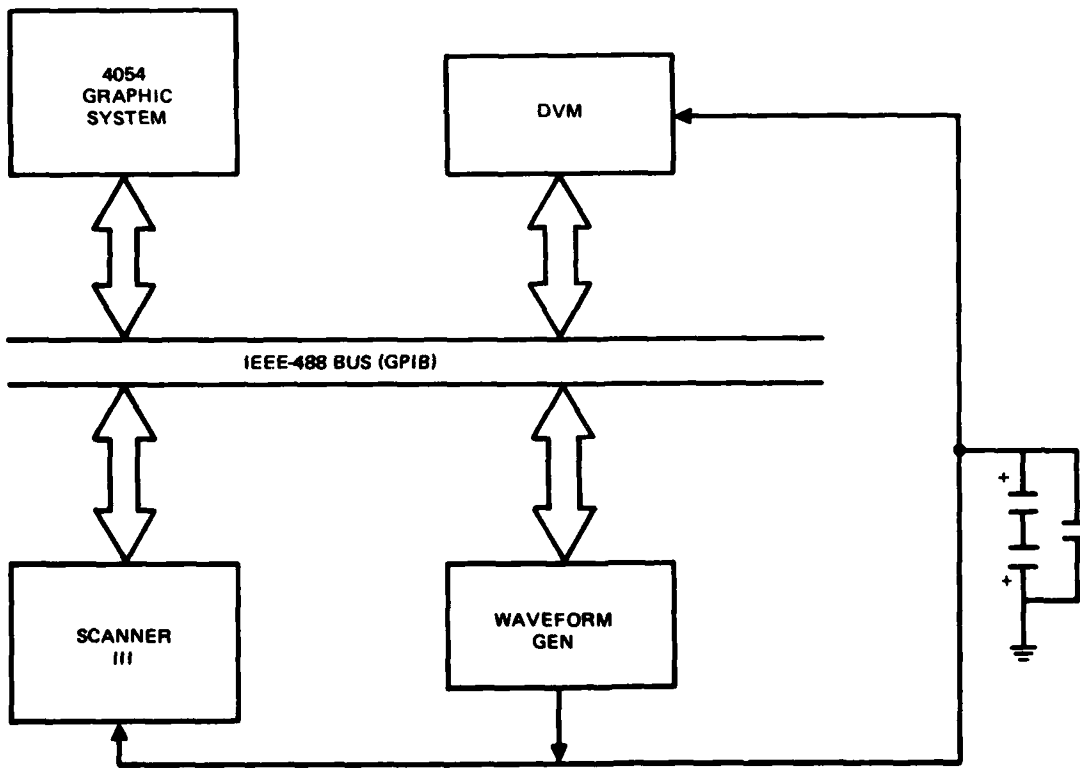


Figure B25. A/D converter test setup.

The first task is to set up the DVM for the appropriate mode of operation. The waveform generator (Wavetek 175A) is then programmed with a slow ramp (about 0.75 mV/s) over the specified input range of the converter being tested. A ramp is chosen because the accuracy of the 175A is specified to be three digits which equates to 10 mV in the 1-volt range. Using a dc offset approach, the inaccuracy exceeds one nominal step size. With a slow ramp, however, a resolution of 1 mV is easily obtained.

Two ramps are programmed, one each for a digital up ramp and a digital down ramp. The protocol is as follows:

1. Sample the DVM output until it equals the nominal voltage for a digital output of zero. Log the voltage at the zero level.

2. Sample the DVM output until it has increased by 1 mV. A check is made to insure against backing up due to transients on the 175A output.

3. Sample the digital output. If it is the same as the previous value or has backed up to a prior value, then return to step 2. If it has moved to the next sequential value, then log the voltage at that value and go to step 4. If the digital output has moved up more than one value, then log one or more levels as having been missed and log the present voltage for the presently returned digital level. In case of this error, the present level being looked at is revised to reflect the last returned digital value.

4. Check that the digital ramp has been completed. If it has not, then go to step 2 and continue.

The software previously used for A/D testing was upgraded significantly to perform these tests. The control was revised to cause acquisition of single pels via the GPIB rather than via the majority of the ICAS data path. This allows a much faster response, which results in less chance for erroneous voltage readings. For the same reason, the ramp was slowed to insure that a sample was taken at each millivolt step. The graphic output software was upgraded to allow output to a digital plotter in any of five size/format combinations, easing the production of report-quality graphics.

TEST RESULTS

Prior use of this procedure was for testing of the Phoenix Data 6-bit A/D converters as well as a single TRW 8-bit converter, using only the six most significant bits. Because these tests were at 6-bit resolution, the nominal step sizes were fairly large, ie 62.5 mV and 30 mV, respectively. This means that a few millivolts of noise would not have a devastating effect on the results.

During the latest test it was determined that the waveform generator is somewhat unstable and, with system noise combined, there is as much as 3 mV of

noise on the analog input to the converter being tested. In previous tests, this was only about 5% (or 10%) of a nominal step size. For the latest test, at 8-bit resolution, the nominal step size is about 7.8 mV, with the noise level at about 40% of that amount. The error characteristics for two separate executions of the test on a single A/D are shown in figures B26 and B27. Figures B26a and B27a show the characteristics for a positive input voltage ramp, while figures B26b and B27b show the characteristics for a negative-going ramp. The envelope of these curves indicates that there is, on the average, a +/- 1 least significant bit (LSB) error, which is considered good. However the average level of the envelope of the characteristic is seen to vary on the order of +/- 10 millivolts. Because it requires about 40 minutes to produce one of these error characteristics, it is believed that the buffer amplifiers surrounding the A/D converter, or possibly the converter itself, may be drifting with time. In addition, substitution of the buffer amplifiers has shown differing results.

Figures B28 through B30 show sample characteristics for the other three TRW converters currently held for project use. Because of the variation in characteristics, it is impossible to be sure how well two or more converters can be aligned for multichannel operation. For this reason, investigation into the causes of the differences in the error characteristics will be continued. The sources of the circuit drift will be investigated as will be the reliability of the test procedure itself.

A possible modification to the test procedure requires a visual observation of indicators showing the bit turnovers. At the (subjective) 50% duty cycle point between two levels on a ramp, a key on the 4054 can be pressed to cause the present voltage to be sampled and logged as the transition point to the new level. It is believed that this will provide a relatively consistent sample point within each level, as shown in figure B31.

Using the present procedure, the voltage used for the transition point to a given level is that voltage at which the first sample at the given level is detected. This means that the voltage logged could be anywhere between point a and point c (on figure B31) or, although unlikely, could be missed altogether. The proposed procedure would place the sampled voltage in the area of point b, where there is roughly a 50% duty cycle and the chance of deviation is much lower.

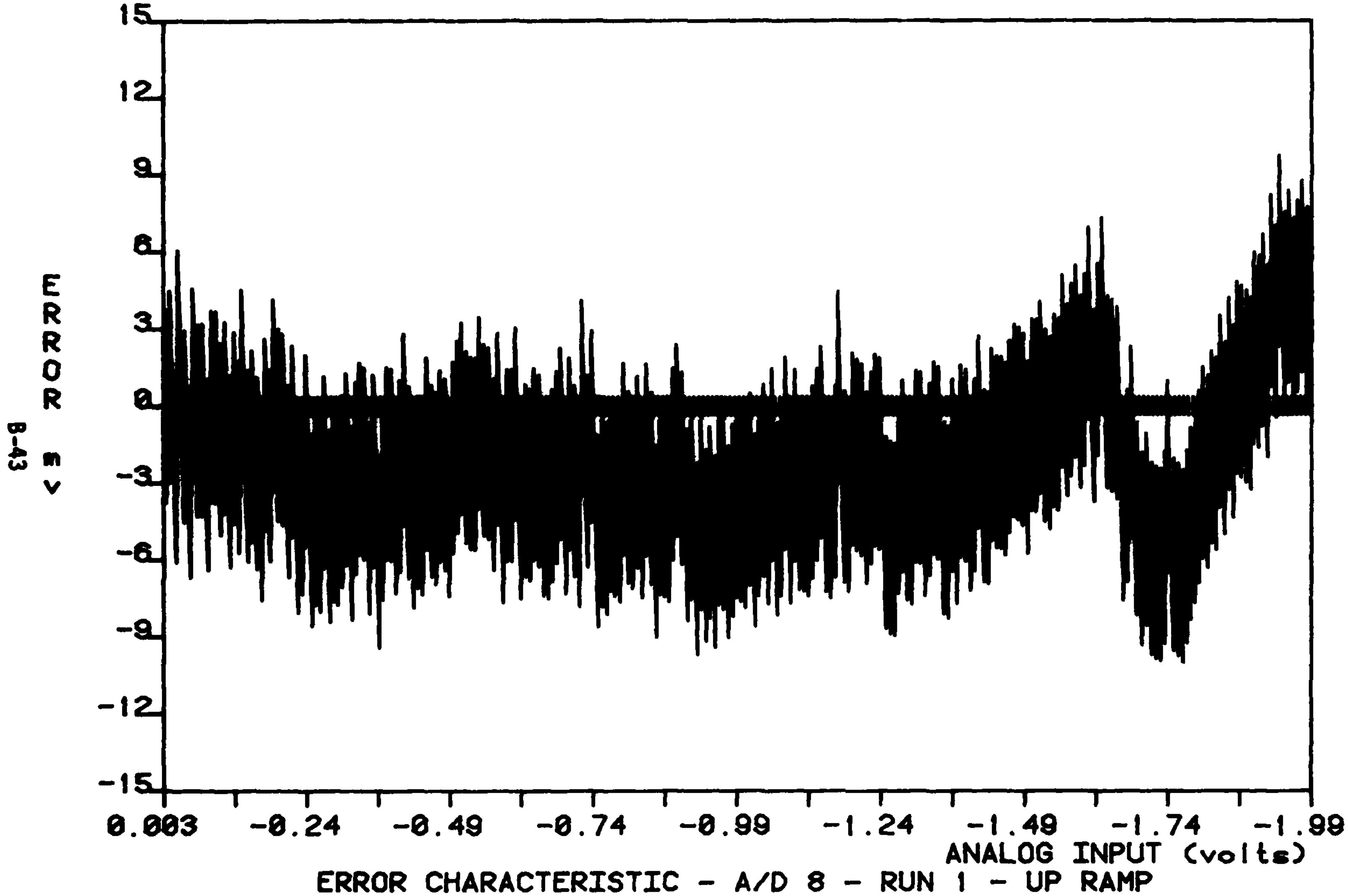


Figure B26a. Error characteristic: A/D 8, run 1, up ramp.

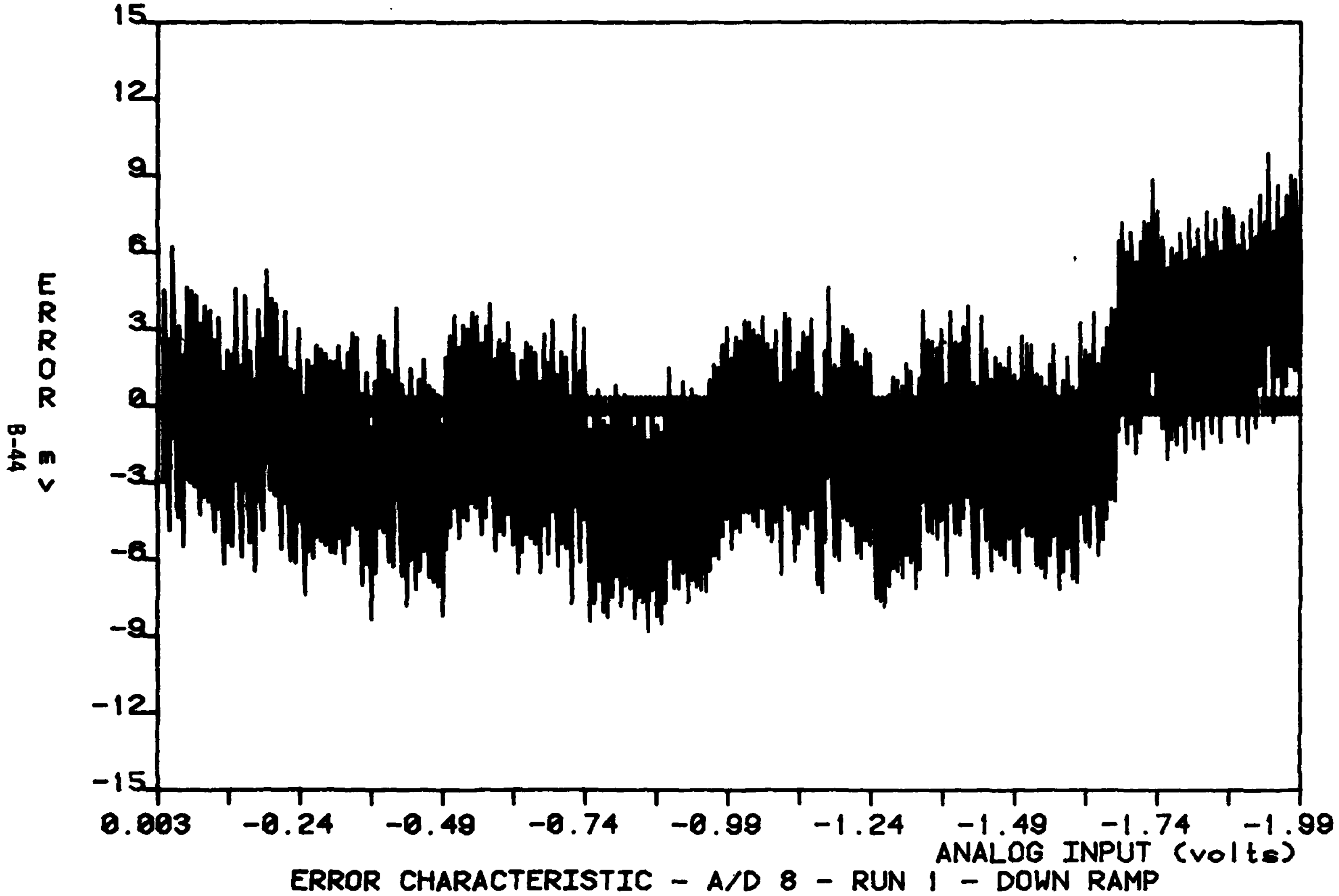


Figure B26b. Error characteristic: A/D 8, run 1, down ramp.

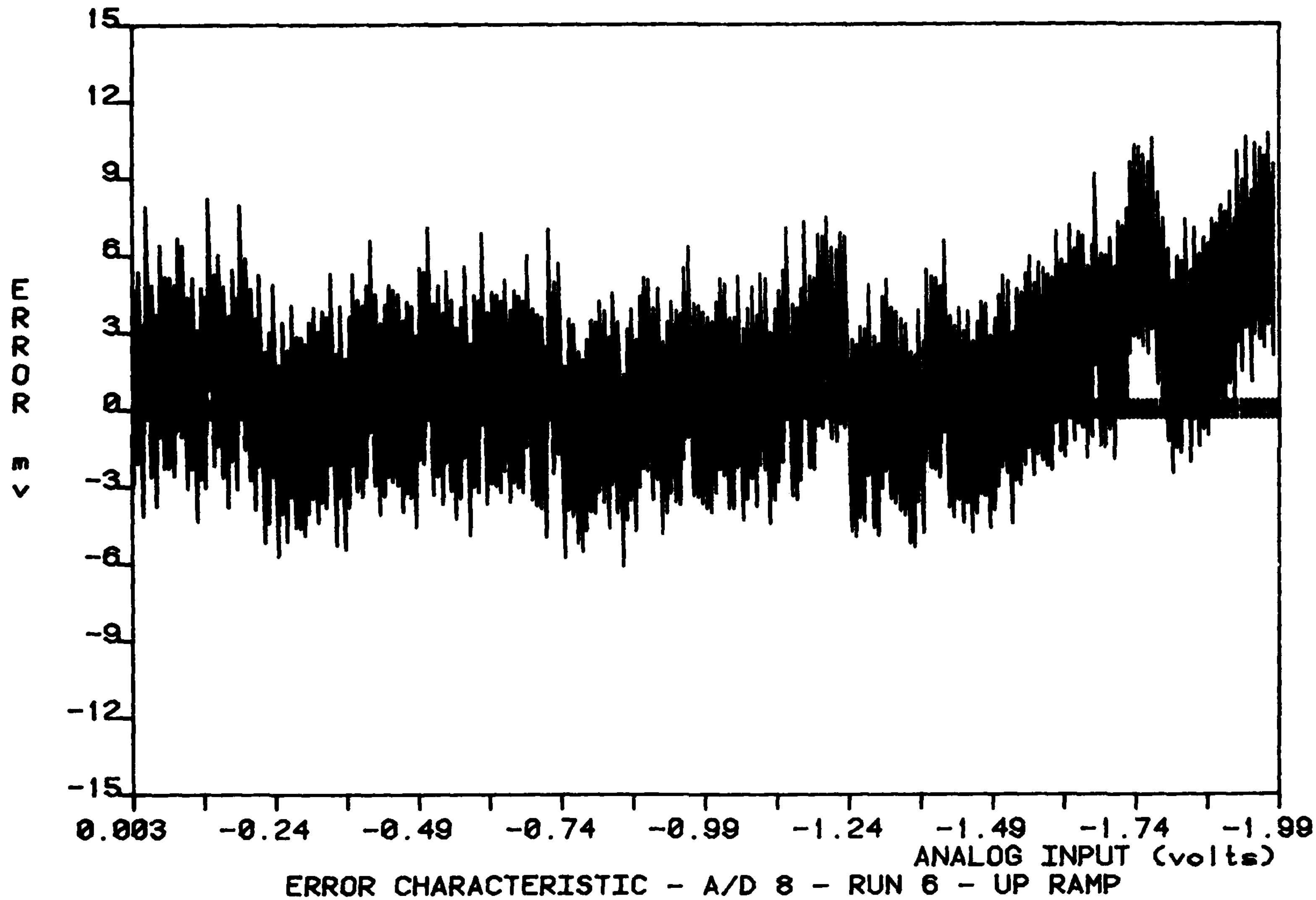


Figure B27a. Error characteristic: A/D 8, run 6, up ramp.

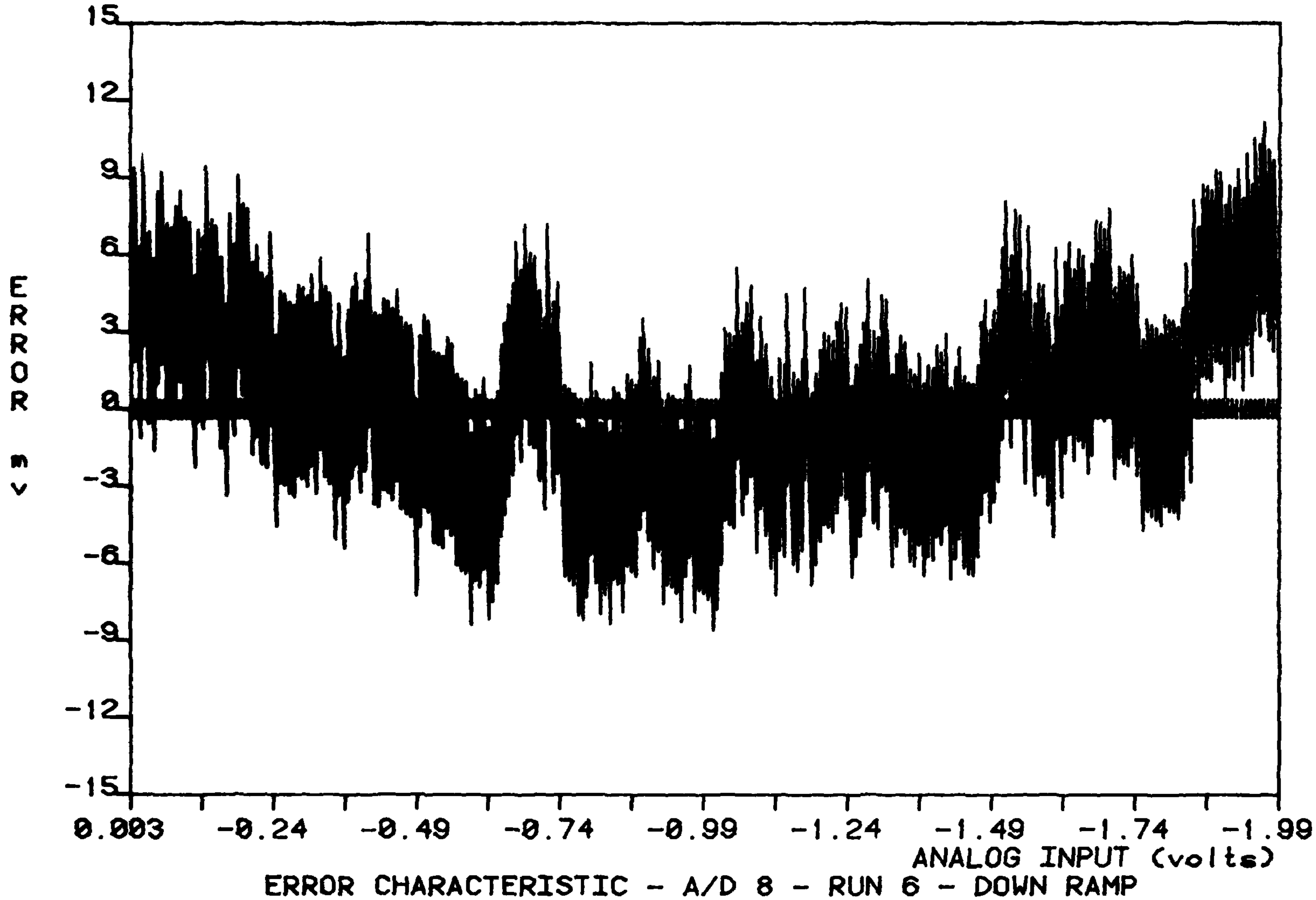


Figure B27b. Error characteristic: A/D 8, run 6, down ramp.

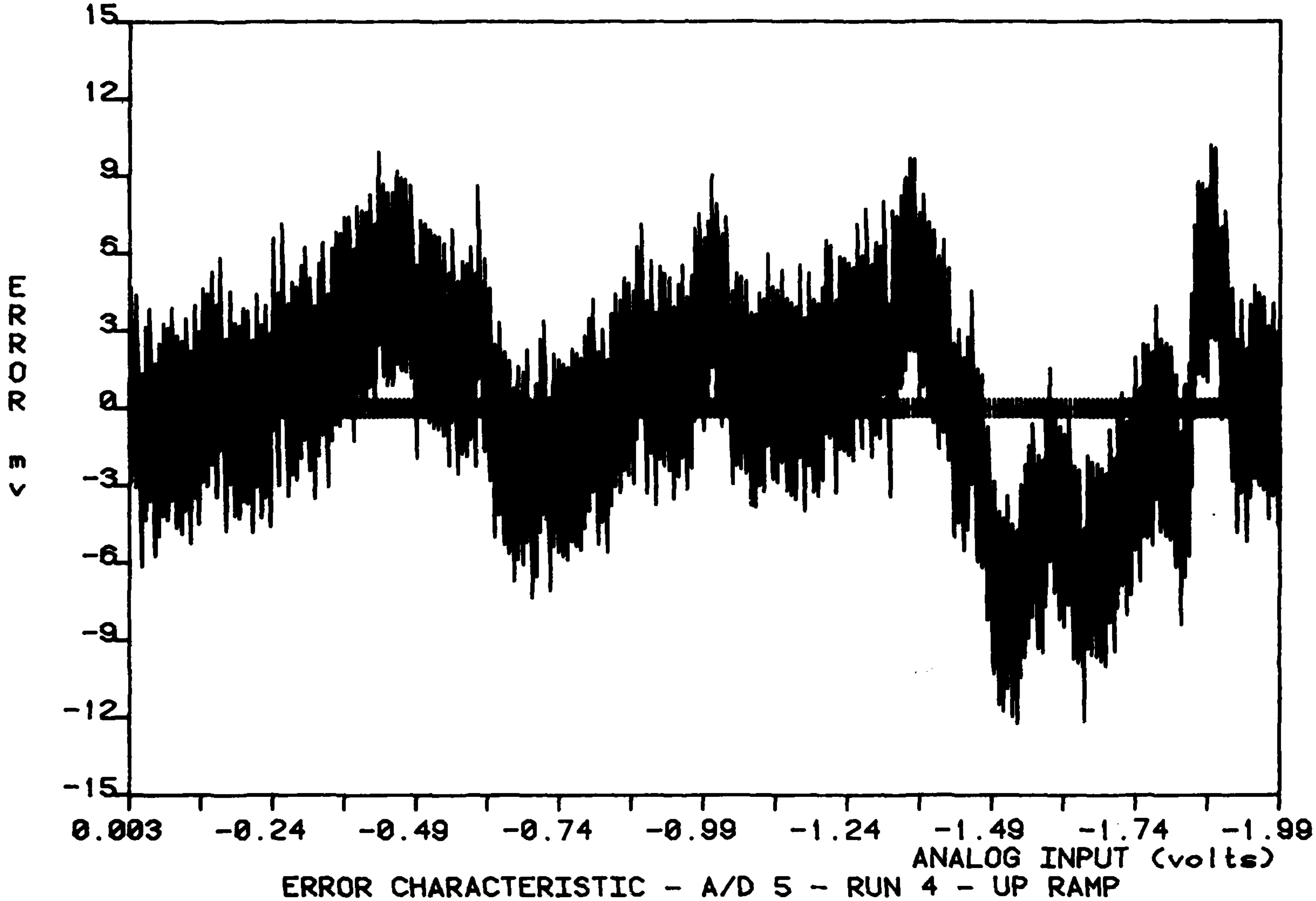


Figure B28a. Error characteristic: A/D 5, run 4, up ramp.

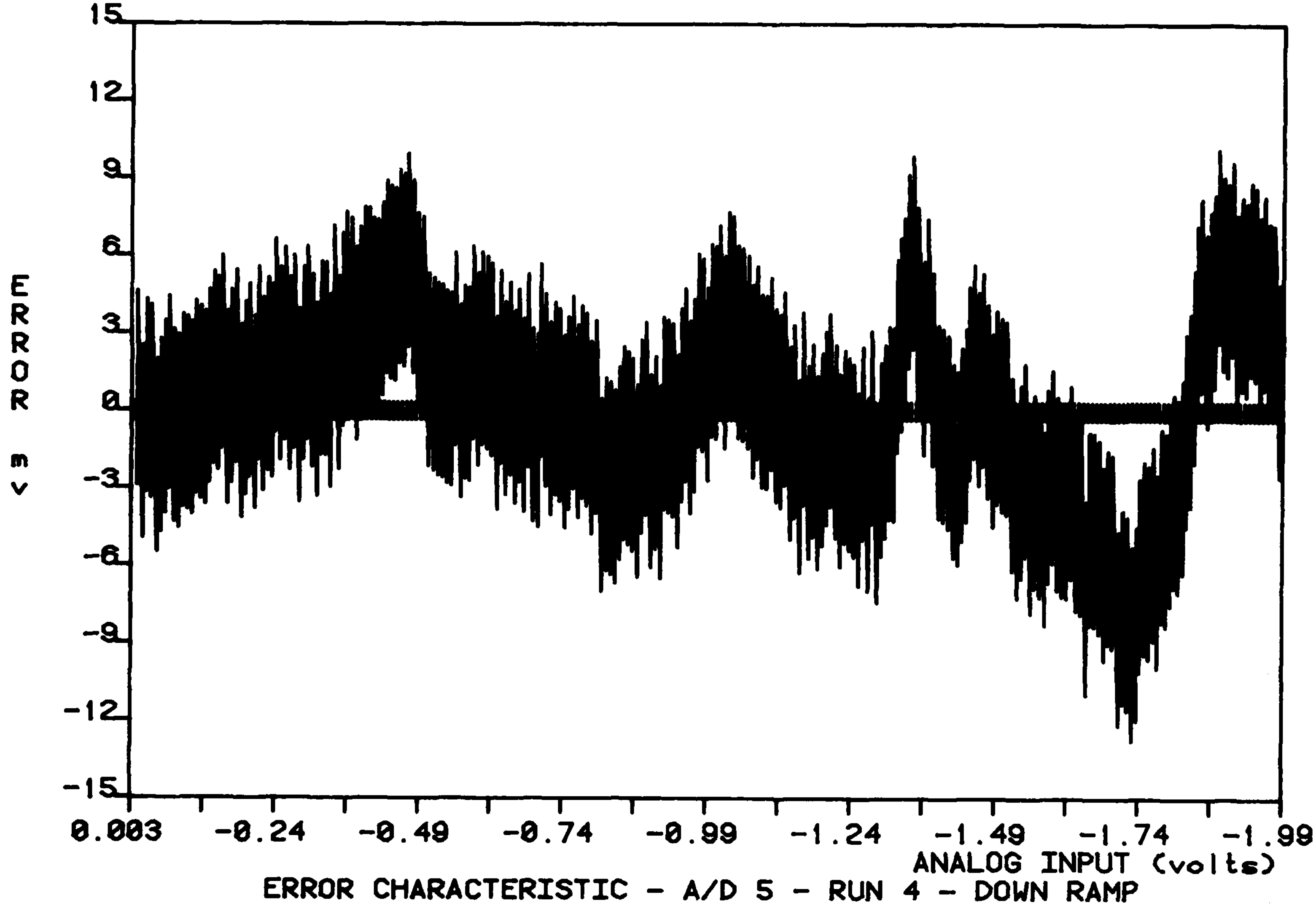


Figure B28b. Error characteristic: A/D 5, run 4, down ramp.

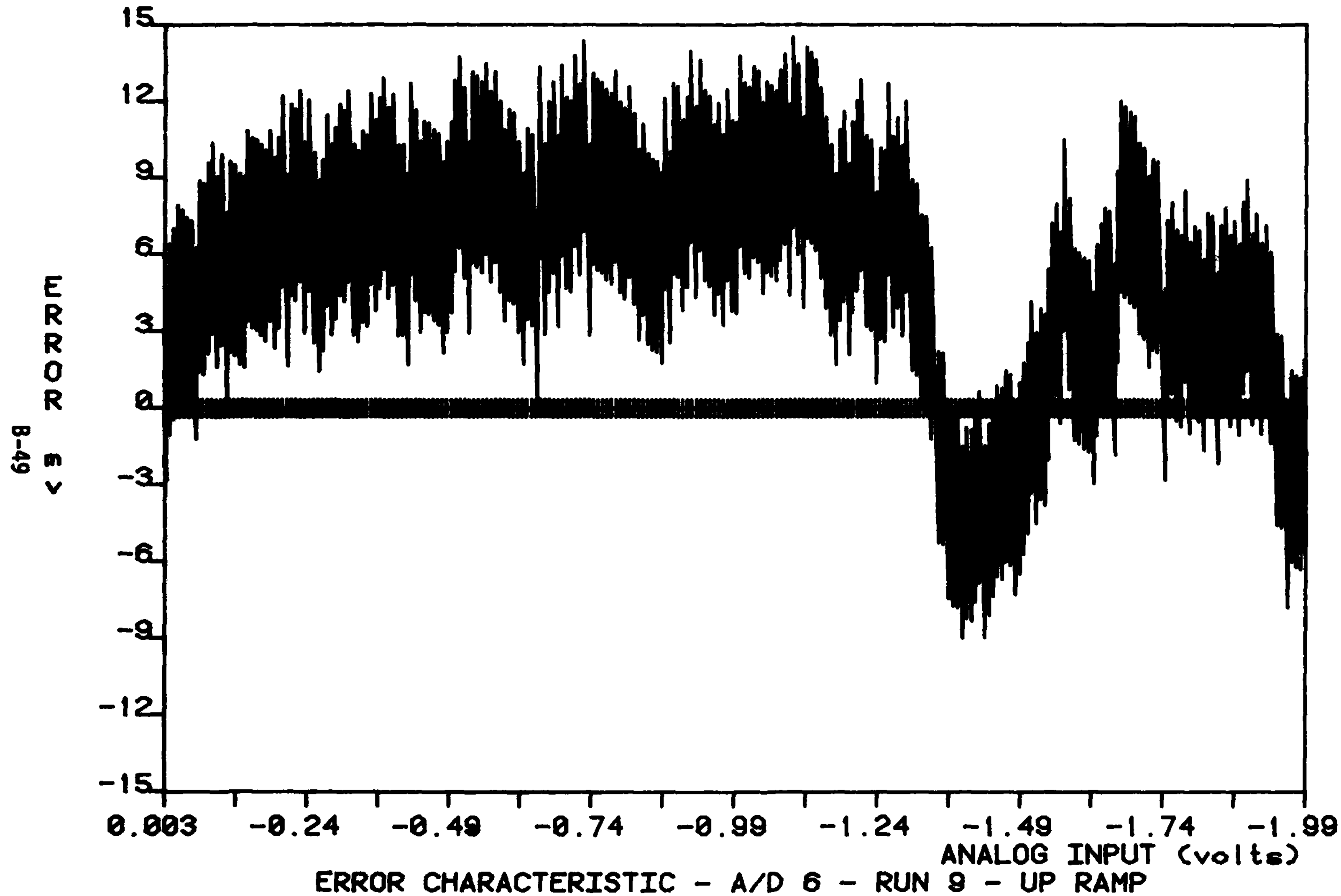


Figure B29a. Error characteristic: A/D 6, run 9, up ramp.

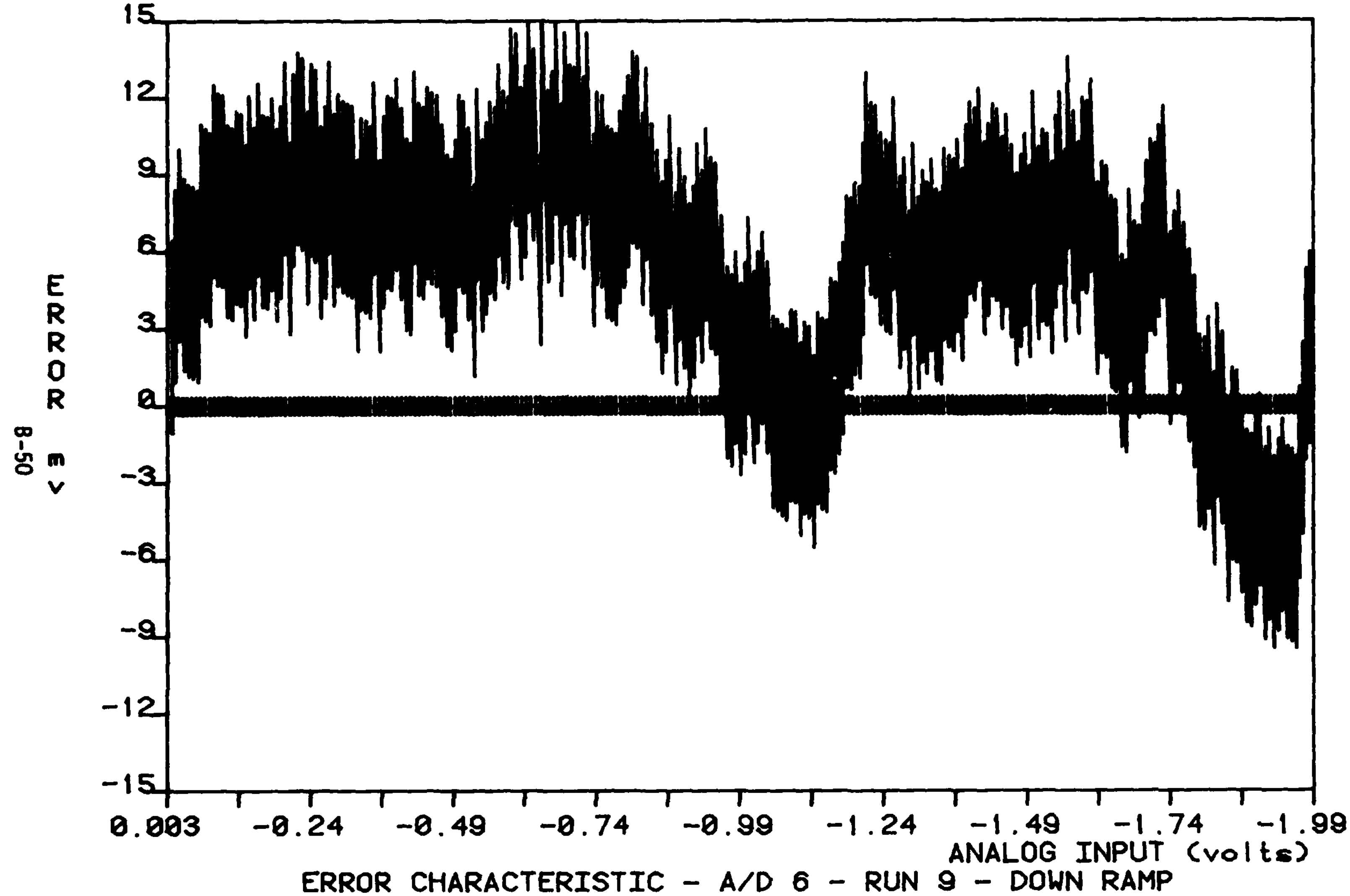


Figure B29b. Error characteristic: A/D 6, run 9, down ramp.

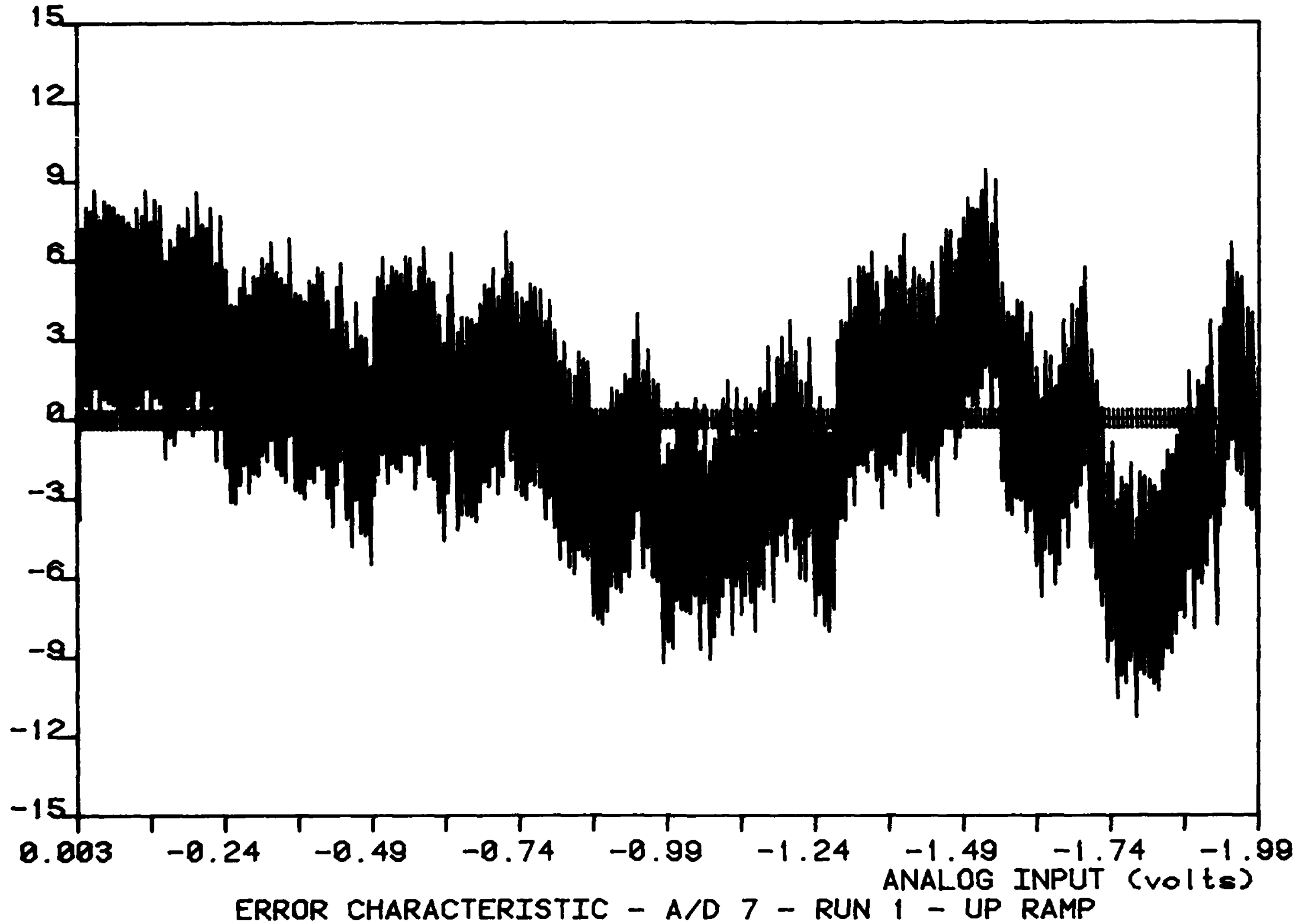


Figure B30a. Error characteristic: A/D 7, run 1, up ramp.

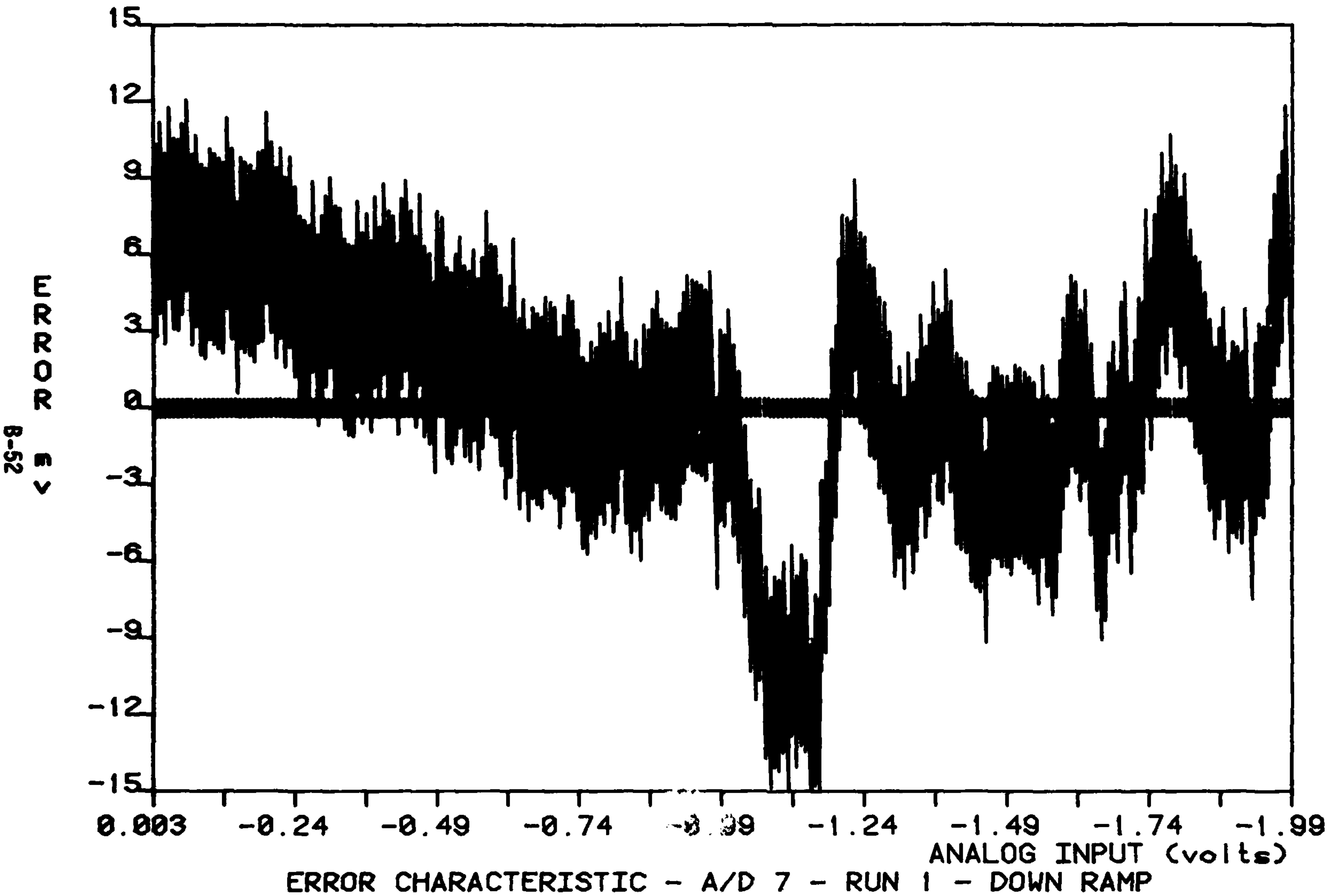


Figure B30b. Error characteristic: A/D 7, run 1, down ramp.

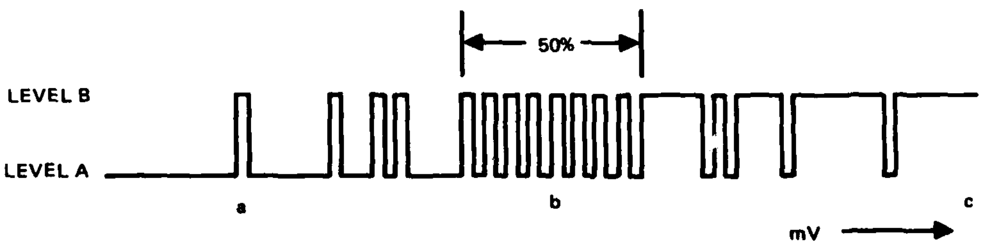


Figure B31. Test procedure sample point.

TDI IMAGER EVALUATION

The US Postal Service awarded contract 104230-79-Z-1613 to RCA Laboratories, Princeton, New Jersey on 18 July 1979. This, the second of two contracts, allowed continued development of a charge-coupled device (CCD) page reader. The device contains 96 rows of 748 photosites each, operating in the time-delay and integration (TDI) mode. Pursuant to the contract, RCA delivered to NOSC two functional TDI page readers for evaluation with another eight still due.

RCA has demonstrated four working TDI imaging devices to NOSC and USPS. The best of the four devices does look quite promising for high-speed scanning applications. Without a frame-store memory in which to store a full image, it was decided that RCA would not attempt to operate the imager in the TDI mode at this time but would, instead, wait for results from NOSC testing in that mode. RCA did demonstrate imager operation in the strobed mode with very good results. The resultant image is shown in figure B32. This photo was taken

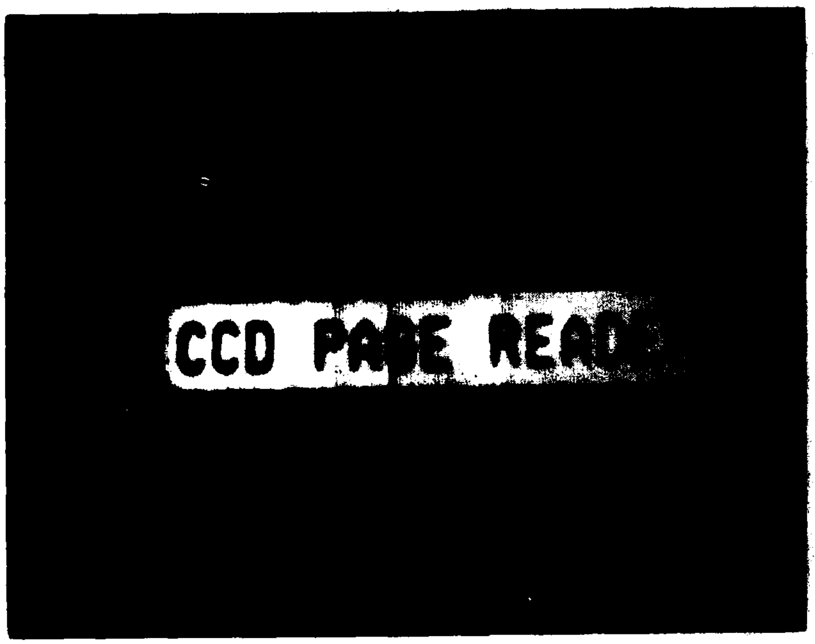


Figure B32. TDI test image.

from a CRT operating in a standard 525-line TV format. The strobe light was synchronized to flash at a 60-Hz rate, equivalent to the field rate of the CRT. The strobe light flashes the image onto the imager, then the image is shifted out of the imager with no further light integration. The video signal input to the CRT was comprised of the summation of two of the output channels from the imager. Thus the image shown contains only 187 pels per line. No additional processing of the analog signal was done. The output data rate for these tests was 4.4 MHz.

The driver electronics for the TDI imager have been completed and are fully operational at RCA. Figures B33, B34 and B35 show the major components of the test setup at RCA. In figure B33 can be seen the CRT monitor, which is used with the COSMAC microprocessor directly above for generation and control of the TDI waveform information, and the RAM boards for storage of the TDI waveform data. Mounted on the scanner table behind the lens is the TDI mounting board with the modular clock driver and video amplifier boards plugged into it. Figure B34 shows the rear of the test setup including the high-speed clock driver board, and figure B35 shows a closer view of the mechanical mounting assembly. RCA has fabricated a partial set of the pc boards along with a duplicate mechanical mounting assembly for NOSC to use in testing the TDI imagers. The set of boards does not include the microprocessor or the RAM boards, since NOSC has fabricated the digital control and RAM memory to be compatible with ICAS. The pc boards and mechanical mounting assembly have been delivered to NOSC, two working imagers have already been delivered to USPS/NOSC, and eight more imagers are due as contract deliverables.

At NOSC the digital control board, the RAM memory board, and the analog processing boards are complete and have been interfaced with the RCA boards. The digital control board contains an interface to the General Purpose Interface Bus (GPIB) that allows control of the scanning operations and loading of the waveform data into the RAM for driving the imager. The RAM board contains storage for 20 waveforms, a phase-locked loop (PLL) circuit for synchronizing the drum speed to the clocking of the TDI section of the imager, and the clock generation and control circuitry. To amplify and digitize the four channel outputs from the TDI imager, two analog processing boards are being used. Each is similar to the one used for the CCD 143 imager. The 2-channel video amplifier section has been reproduced in pc form, one being used on each analog board. The A/D converter section as used for the CCD 143 has been modified to include a T/H amplifier to remove clocking transients from the analog signal. It has also been reproduced in pc form, and two of these boards are used on each analog processing board. Each of the four analog outputs from the TDI imager is amplified and digitized separately, then transmitted to the personality chassis where the four pel streams are properly formatted for storage in memory with either 6 bits per pel or 8 bits per pel.

Initial testing of the TDI imager at NOSC is under way and consists of verifying operation of the imager in the strobed mode. This test will also be used to assess the uniformity of response of the entire array of photosites.

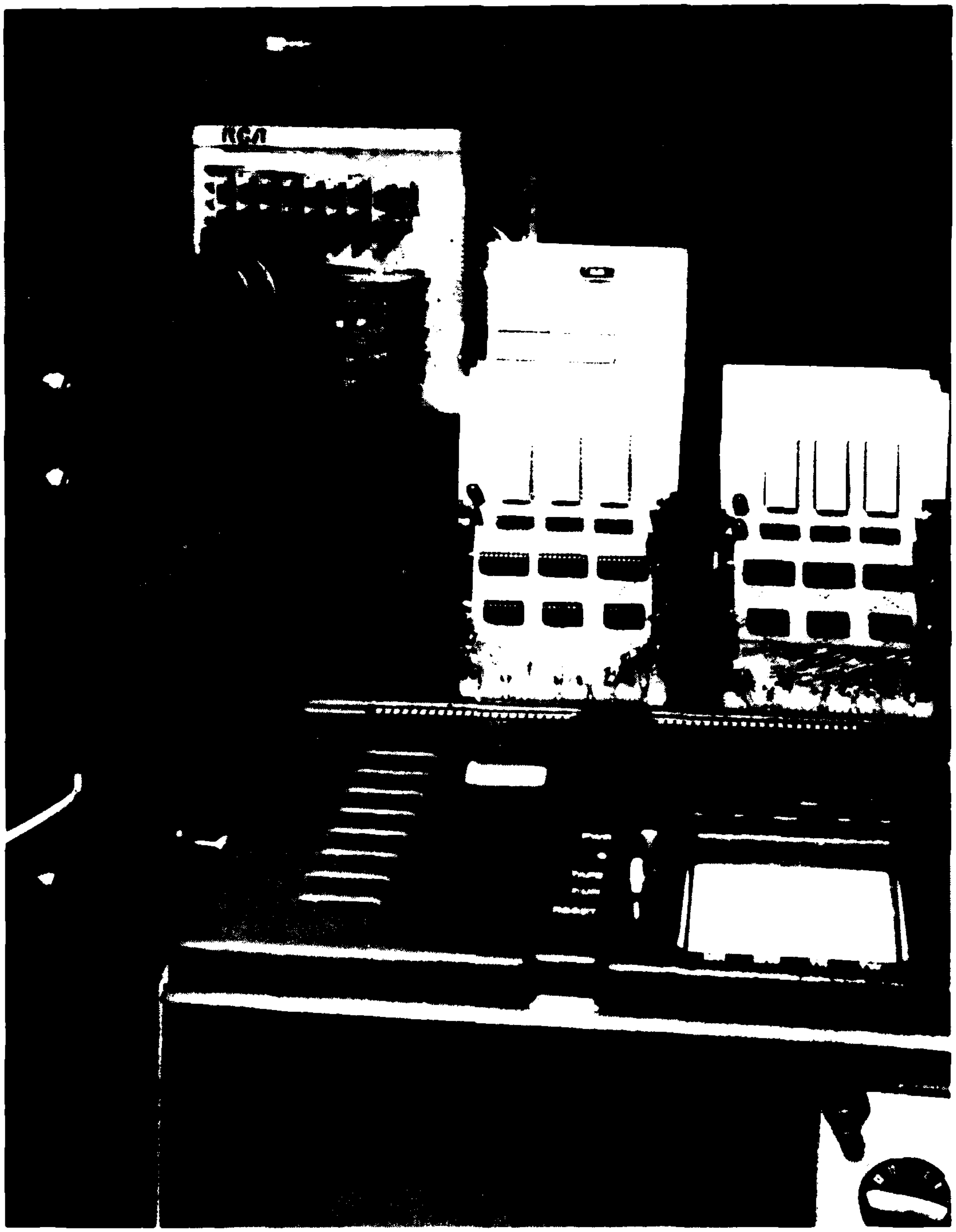


Figure B33. TDI test setup – front view.

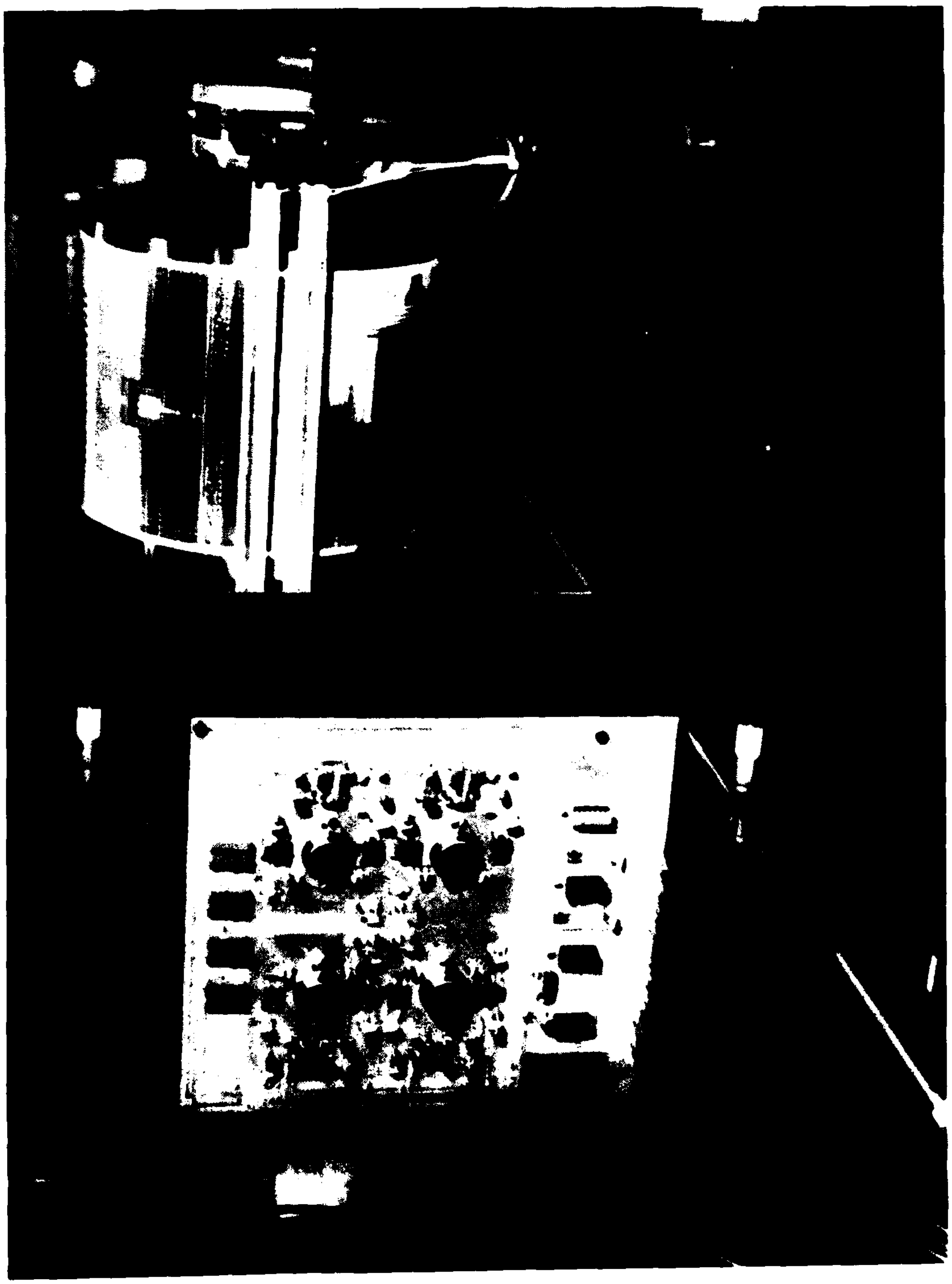


Figure B34. TDI test setup – rear view.

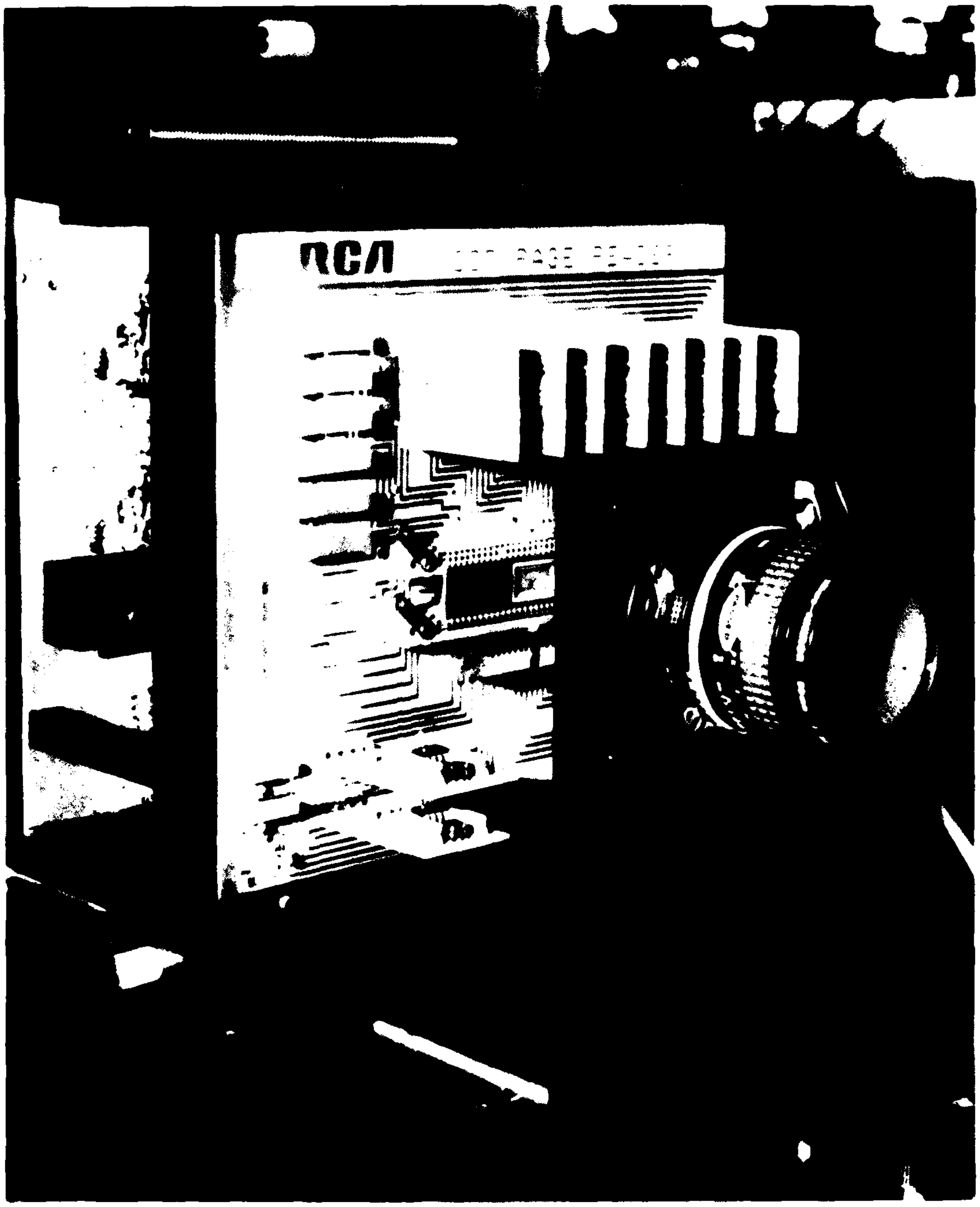


Figure B35. TDI mechanical mounting assembly.

Following that test, the attempt will be made to operate the imager in the tracking, or TDI, mode. Operating parameters to be tested with the imager operating in that mode include dynamic range, sensitivity, tracking accuracy, maximum operating rate, and linearity.

The TDI Imager Interim Report (contained in reference B1), describes in detail the TDI device and its support electronics. The balance of this section describes the results of test efforts to date.

TEST RESULTS

To date, neither TDI page reader has been successfully operated at NOSC. The first of the two devices was damaged and has since been repaired by RCA. With the second device, however, the following demonstrations have been made:

- Operation of the on-chip output amplifiers.
- Charge injection into the output shift registers.
- Response of the output registers to a small spot of focused light.
- Response of at least part of the TDI array to strobed images and transport of the resulting charge to the output amplifiers.

Figure B36 is taken from reference B2, which describes the TDI device. It shows a schematic layout of the TDI array and the onboard 3-stage source-follower output amplifier. To test the output amplifiers, all input clocks are removed. The floating diffusions (marked FD1, FD2, FD3, FD4, and FDref in figure B36) are isolated from the output registers by setting the ϕ_{out} gate to -10 V. These diffusions are connected to the reset voltage, V_{RS}, by setting the reset gate ϕ_{RS} to +10 V. Thus V_{RS} is the input to each of the five output amplifiers. The source-follower outputs were loaded with the 5k-ohm scope probe used. Figure B37 shows the channel 1 output response. The other amplifier responses are similar.

To test the output register, the clock inputs ϕ_1 through ϕ_8, M1 through M7, and S2 through S4 are removed. The output register is isolated by setting clock inputs T04, 402', and 404' to -10 V. The high-speed clocks 401, 401', 402, 403, 404, O_{RS}, and O_{out} are applied. To allow charge injection, the gates G1 and G2 are grounded.

Charge injection and the response of the output register to a small focused light spot have been demonstrated simultaneously as follows. The high-speed clocks are disabled for 9/16 of the TDI period and are enabled for the remainder. As currently configured, the high-speed clocks run at 2.625 MHz and the TDI period is 97.5 μs. Thus, the clocks are disabled for 54.8 μs and enabled for 42.7 μs. While the clocks are disabled, a small spot of light is focused on a few potential wells in the output registers and charge accumulates in these wells. Simultaneously, charge is being injected via V_s and V_s' if these source voltages are less than about 8 volts. After the clocks are turned on, and after some delay, the injected charge and the photon-induced charge are manifested at the chip outputs as negative-going

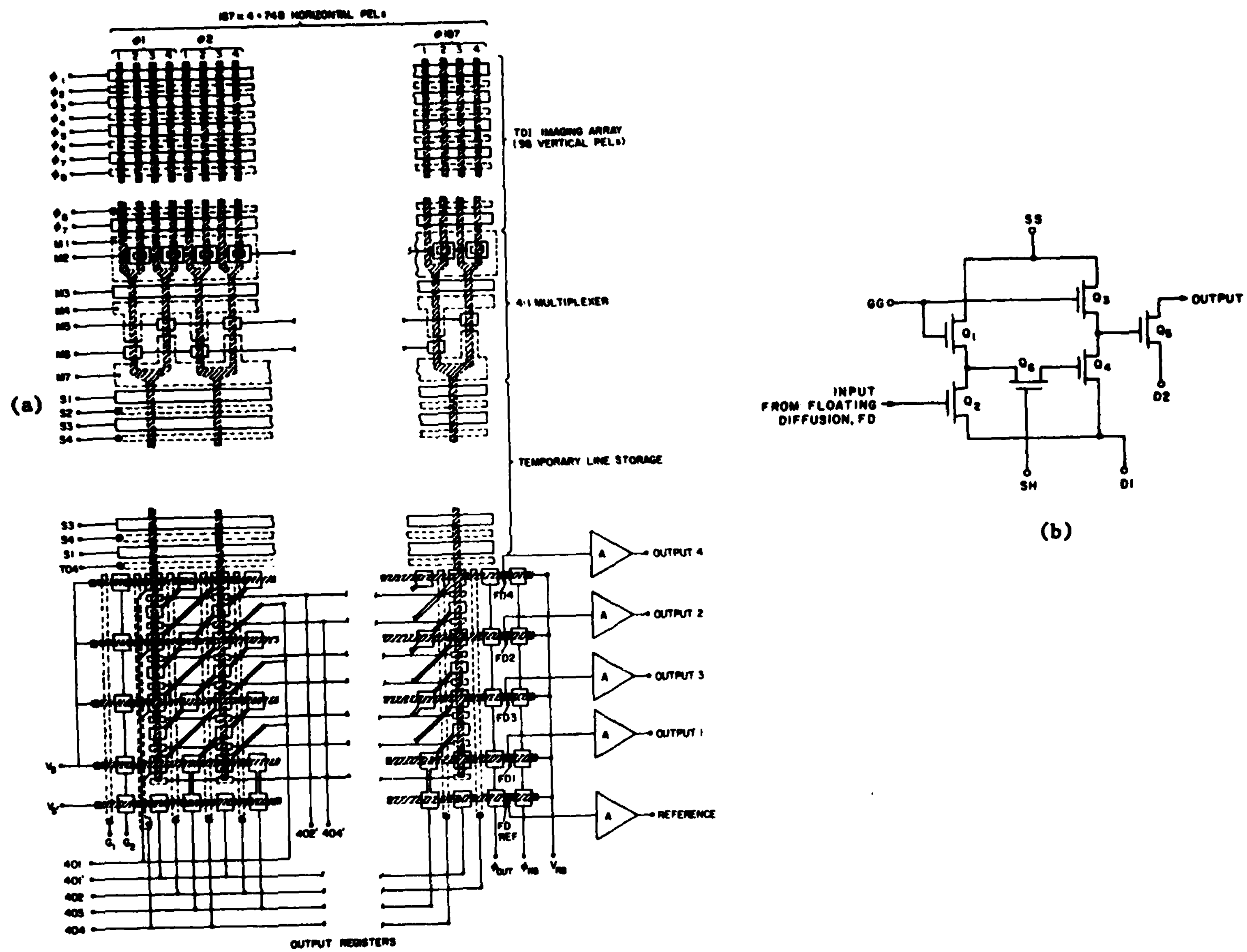


Figure B36. Schematic layout and output amplifier circuit. (a) 748- by 96-element array with four-phase electrode-per-bit clocked TDI array and 4:1 multiplexed output. (b) Three-stage source follower output amplifier.

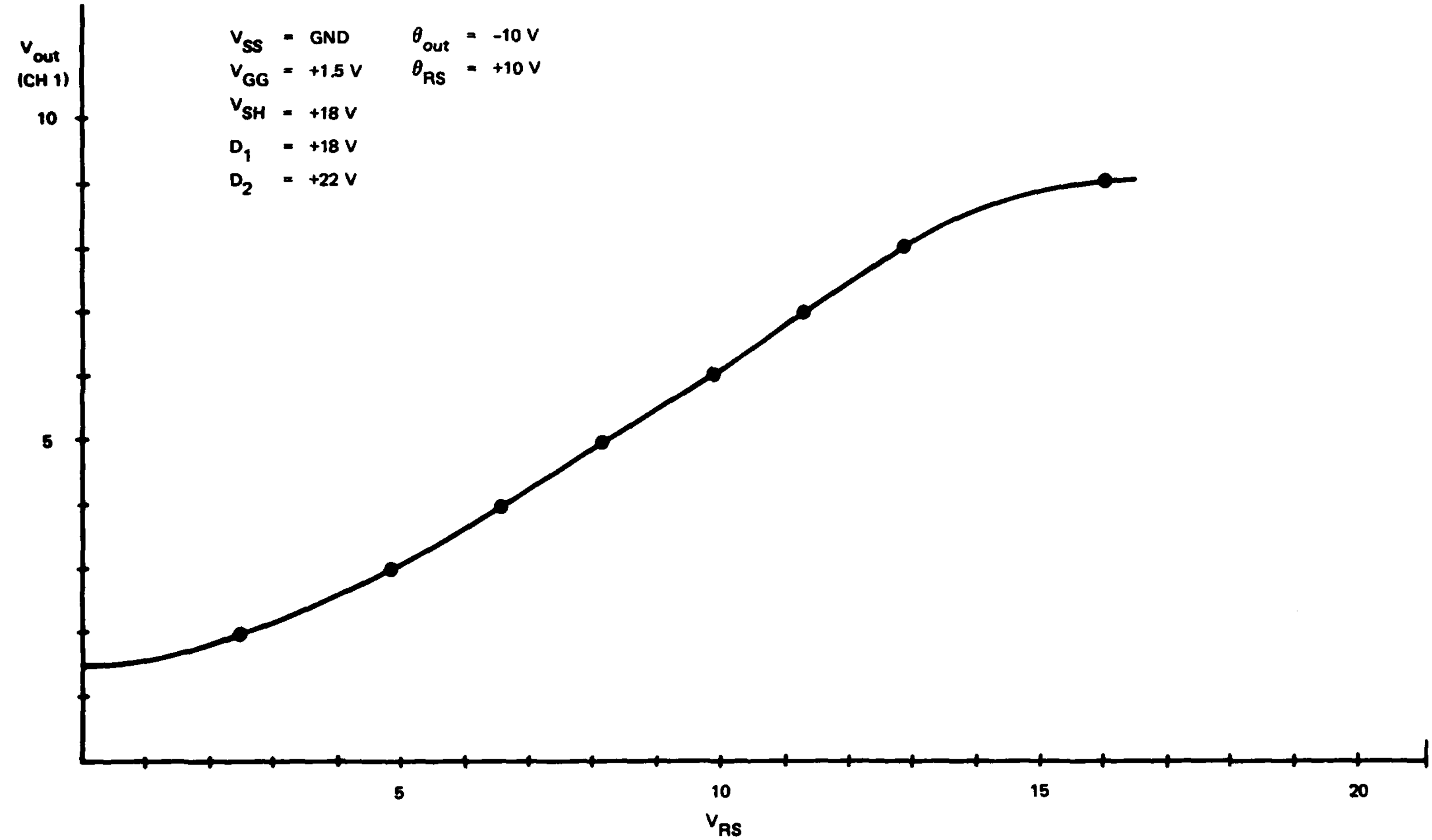


Figure B37. TDI channel 1 output amplifier response.

signals of about 200 mV maximum. Figure B38 shows the channel 1 through 4 outputs when clocks are active. The first two pulses in the upper two traces result from the light spot falling on output registers 3 and 4. The position of these pulses and the channels in which they occur can be controlled by moving the light spot on the output registers. The magnitude of these pulses is controlled by changing the intensity of the light spot. But the fact that the magnitude of the pulses is not a function of the position on a particular output register is an indication of reasonable charge transfer efficiency.

A second set of pulses is found on all four output channels, as shown in figure B38. These pulses are the result of charge injection at V_S and V_S'. Their positions are fixed since they always appear after 187 clock pulses, ie the number of pels in the output register. Their magnitude is controlled by V_S and V_S' over a narrow range of voltage near 8 V. Above this range, no charge is injected. Below it, all output pels are saturated.

To demonstrate chip operation, the image of a test chart is focused on the TDI array. The chart is illuminated with a strobe flash upon receipt of a command over the GPIB interface. When the control circuitry receives a strobe command, it holds all clock inputs at their initial state for about 100 μs. Within this period, the strobe is flashed. The TDI clocks are then enabled and the charge is clocked to the output amplifiers.

Two operational modes are possible. Strobe commands can be issued repetitively, allowing the 4-channel video outputs to be observed on an oscilloscope, pel by pel and line by line. Figure B38 shows one such line. Alternatively, a single strobe command can be generated and the resulting video data can be digitized, stored in memory, and displayed.

Images of a horizontal bar pattern have been captured and displayed. Figure B39 shows the oscilloscope traces of the four channels during the acquisition of the bar pattern. Figure B40 is a photograph from the display of the acquired image. While these images are very crude, they indicate

Photosensitivity of the TDI array with some horizontal resolution.

Transport of the charge down through the TDI array and multiplexer and into the temporary storage registers.

Transfer of charge from the temporary storage registers into the high-speed output registers.

In addition, evidence of some vertical resolution has been observed. With a V-shaped symbol focused on the array, the spatial separation of the line-by-line response as observed on the scope is found to decrease as the line position moves down the V.

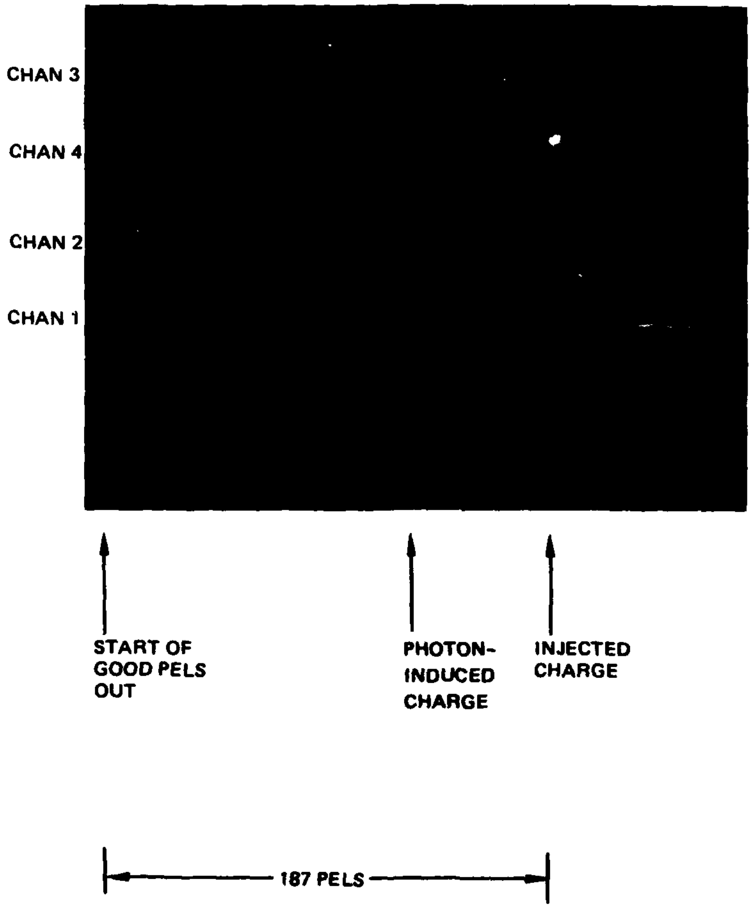


Figure B38. Demonstration of charge injection and photosensitivity in output registers.

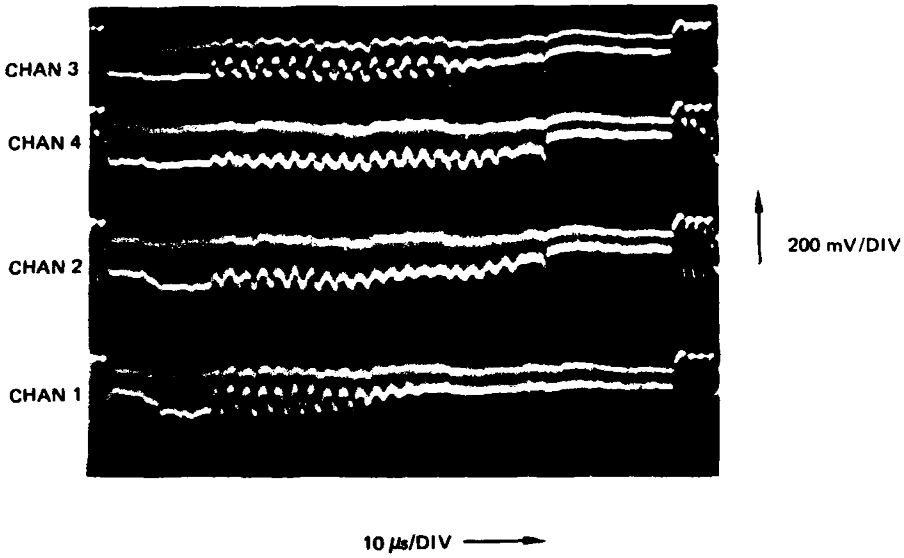


Figure B39. Sample line from bar pattern image.

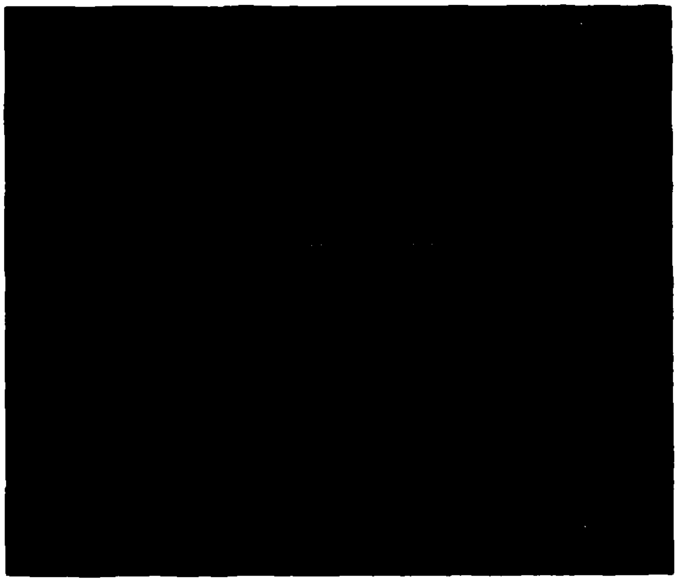


Figure B40. Display of bar pattern image (64 lines by 748 pels).

Major problems remain, however. Among these are the following:

The TDI array saturates when the transport clocks to all 96 rows of photosites are enabled. Reasonable operation has been realized only by enabling only the lower 32 rows.

For a given line, sensitivity varies from channel to channel. An exposure level high enough to stimulate a less sensitive channel often saturates another. This effect causes the pel brightness of a captured image to vary across a line with a period of four pels.

Sensitivity varies from line to line down the array. Typically, some lines must be saturated to elicit a response in others. Thus portions of the captured image appear washed out.

At this point, it is believed likely that some fundamental misadjustment of chip inputs exists, accounting for the anomalies observed.

FUTURE PLANS

The RCA TDI page reader has some 30 clock inputs, most with unique amplitudes, bias levels, and waveforms. In addition, the chip requires several dc voltage levels. The proper relationship between all inputs is required to enable the charge packets to move from the TDI array to the output amplifiers. The specification of these inputs is complicated by the lack of intermediate observables. The only outputs that can be monitored directly are those from the output amplifiers themselves.

Discussions with RCA personnel have increased the understanding of the TDI device operation, especially in relation to interregister transfers and in the development of a procedure for checking clock timing. This should expedite the correct adjustment of the device inputs. When images of reasonable quality are obtained, the test plan described in reference 1 is to be executed. The object of these planned tests will be to characterize the TDI page reader as completely as possible.

DOCUMENT CLASSIFICATION

The purpose of the image classification algorithms is to distinguish continuous-tone printed matter from bilevel printed matter. The basic method is to analyze a histogram generated from the values of the individual pels of the digitized images. If there are just two predominant peaks on the histogram and all other values are small, then one can assume that just two useful grey levels exist. The peak at the higher illumination level represents the light background and the peak at the lower illumination level represents the dark ink. The pel brightness histogram (PBS) algorithm has proven to be a useful tool.

Other algorithms have been developed because of a concern that some nonbilevel subjects that have a limited number of pels with values at other than the normal bright background and dark ink levels may pass the pel brightness histogram test. These algorithms are based on the assumption that pages of text are bilevel and that text can be detected by the presence of regular patterns having the same spatial frequencies as typed text. These include the vertical pattern due to a set number of lines per inch and the horizontal pattern due to a set number of characters per inch. The standard tool for detecting such patterns is the fast Fourier transform (FFT). The disadvantage of this test is that bilevel charts and graphs do not look like text and therefore will fail these tests.

The spatial frequency algorithms operate on sums of the pel brightness values either across a page on a line-by-line basis (vertical) or down a page on a pel-by-pel basis (horizontal). These sums are treated as one-dimensional arrays for use by the FFT algorithm. The arrays are partitioned into successive groups of values with starting points at an arbitrarily chosen interval. An FFT is run on each partition, and the resulting power spectrum is checked for the appropriate line or character spacings normally associated with textual-type material.

The number of successive partitions containing the appropriate frequency line in the power spectrum is summed for the "consecutive partitions" test. The total number of partitions containing the frequency line is used for the "total partitions" test. If a document contains two consecutive partitions with the frequency line, the test is considered "passed," yielding a decision that the document is bilevel. If the document contains at least four partitions total with the frequency line, that test is considered "passed," with the same decision.

The vertical spatial frequency algorithm has proven to be of value because virtually all documents have a fixed line spacing throughout the page. Although normal line spacing is six lines per inch, line spacing can vary from three to twelve lines per inch. For example, the closest spacing is commonly found in the boilerplate of legal documents.

	Title	Characteristic
1	WTM letter	Justified
2	WTM letter	Not justified
3	Circuit board	Continuous-tone photograph
4	IEEE FAX chart	Some continuous tone
5	WJM letter	Standard business letter
6	George Washington Univ. letter	Business letter on beige paper
7	"Paul Bunyan" letter	Handwritten letter
8	Personnel Action Request	Form
9	Form 1	Small text
10	Application-type photo	Continuous tone
11	Form 2	Mostly fine boilerplate print
12	Form 3	Completed by hand with several numerical values
13	Form 4	Completed by typewriter with text and numerical values
14	Form 5	Mostly fine boilerplate text
15	Naval or similar message	Form with few lines
16	Form 6	Completed by typewriter with text
17	Computer printout	Turned sideways
18	Form 7	Mostly fine boilerplate text
19	AODC p 1	Raw text, data not corrected with calibration data
20	AODC p 1	Page skewed slightly, text, data uncorrected
21	AODC p 2	Text, data uncorrected
22	AODC p 3	Text, data uncorrected
23	AODC p 4	Text, data uncorrected
24	AODC p 5	Text, data uncorrected
25	AODC p 1	Text, data corrected with calibration test data
26	AODC p 1	Text, skewed, data corrected
27	AODC p 2	Text, data corrected
28	AODC p 3	Text, data corrected
29	AODC p 4	Text, data corrected
30	AODC p 5	Text, data corrected

Table B1. List of document classification test subjects

The horizontal spatial frequency algorithm has less utility than the above algorithms because variable character widths are found in many office typewriters and because spaces are distributed throughout each line by word processors for justification or proportionally spaced typing. This algorithm is still useful as a confirmation test or for locating a continuous-tone image that may be placed in the corner of a page of text.

Table B1 contains the list of subjects used to test the algorithms. It includes not only standard text with and without justification but also text on beige paper and on pages that were skewed slightly when placed in the digitizer. The subjects also included preprinted forms. These are definitely bilevel and should be detected as such, but the combination of small text, lines, and handwritten or typewritten responses is intended to stress-test the algorithms. Three continuous-tone subjects were included. Photographs of an electronic circuit board, of the IEEE FAX chart, and of a man were also included. The first two were included because they have lines that may confuse the FFT algorithms. Plots of some of these are not included, but they were all tested to insure that results chosen for inclusion would be typical and they confirm the algorithms or point to areas for improvement.

Figures B41 through B44 contain pixel brightness histograms of subjects 5, 3, 10, 14, 16, and 4. Figures B41a and B41b show the histogram of subject 5, containing typical text, with a coarse semilog plot and a linear plot, respectively. Figures B42a and B42b contain the histogram of subject 3, a continuous-tone photograph. The form of the histogram is easily distinguished from that of subject 5. This is also true of figure B43 which shows the histograms of subjects 10, 14, and 16 (labeled as images 2, 6, and 8, respectively). The histogram of subject 4 (the IEEE FAX chart), shown in figures 44a and 44b, appears similar to but not identical to histograms of typical text. It was hoped that the low value for the ratio of the primary peak to the secondary peak would be the key in distinguishing text from nontext. The inclusion of the histograms of subjects 14 and 16 makes that difficult, because the greater amount of ink on the preprinted forms precludes the use of a threshold in the middle of a wide gap between bilevel and continuous-tone subjects. No solution to the problem is immediately apparent, but work is progressing in that direction.

Figures B45, B46 and B47 are plots of the vertical spatial frequency test results for subjects 5, 3, and 4. Each point of these plots shows the power in the frequency region near six lines per inch over a 256-pel section (1.28 inches at 200 pels per inch). After computing the power for one section, the starting point for the next section is moved 128 pels, or one-half of the size of the section.

This procedure is able to analyze the entire document and can thus detect those subjects with an isolated portion of continuous tone image somewhere on a page of text. The typical power of text observed thus far is in the region from 58 dB to 65 dB, as demonstrated by the fairly consistent power characteristic shown in figure B45. Most nontext subjects have either a power significantly below the 55 dB level (figure B46) or an inconsistent

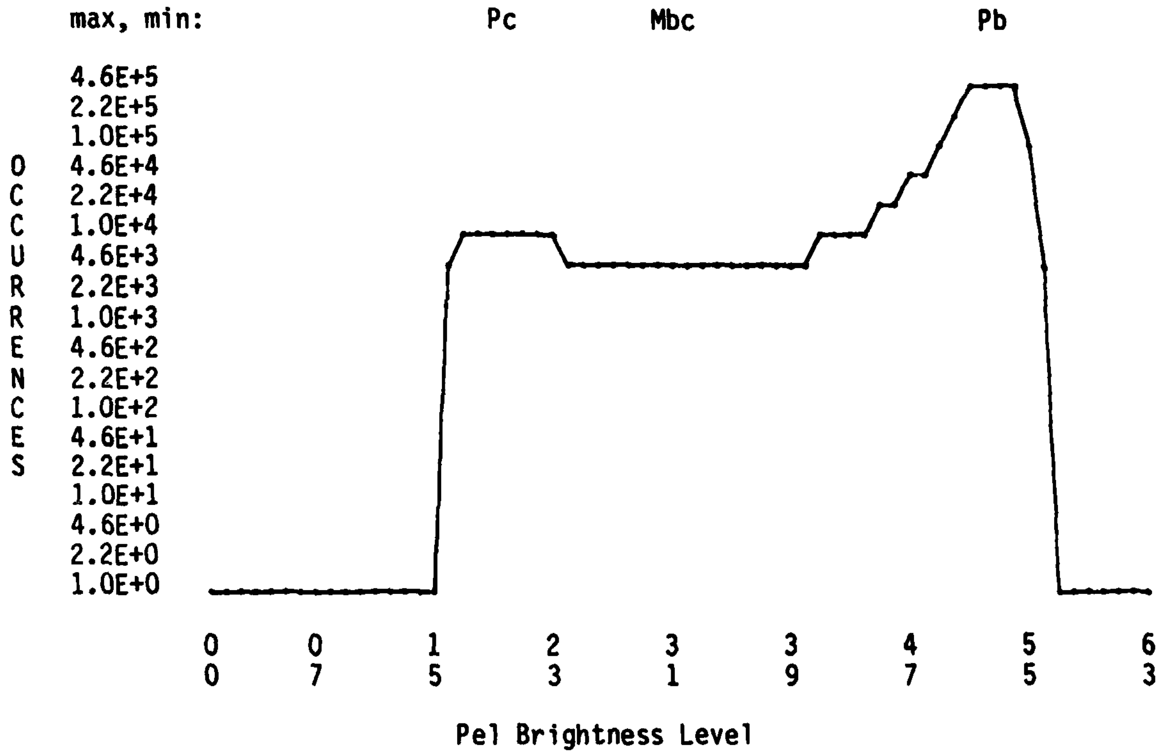


Figure B41a. Semilog plot of subject 5 histogram.

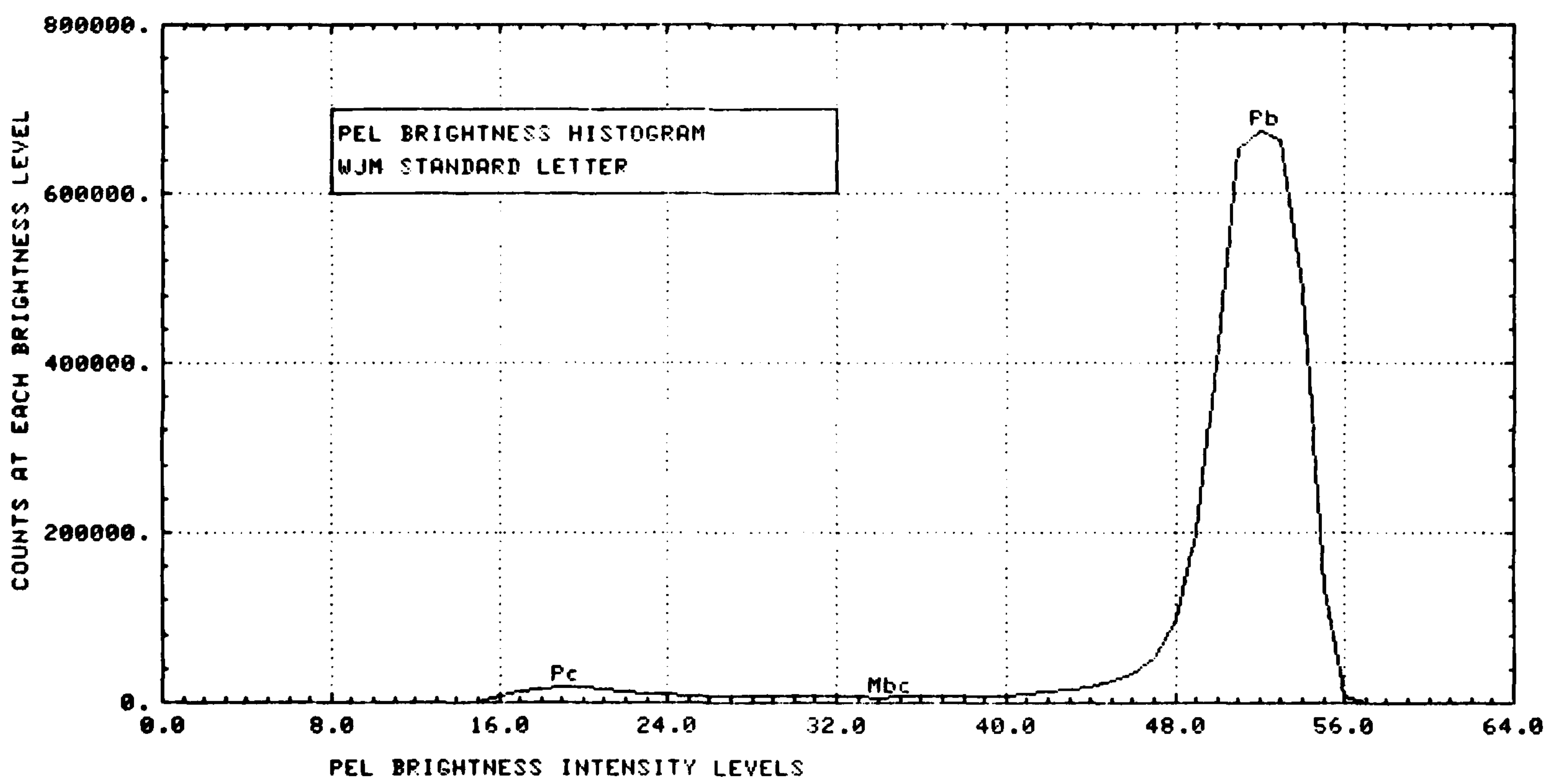


Figure B41b. Linear plot of subject 5 histogram.

Figure B42a. Semilog plot of subject 3 histogram.

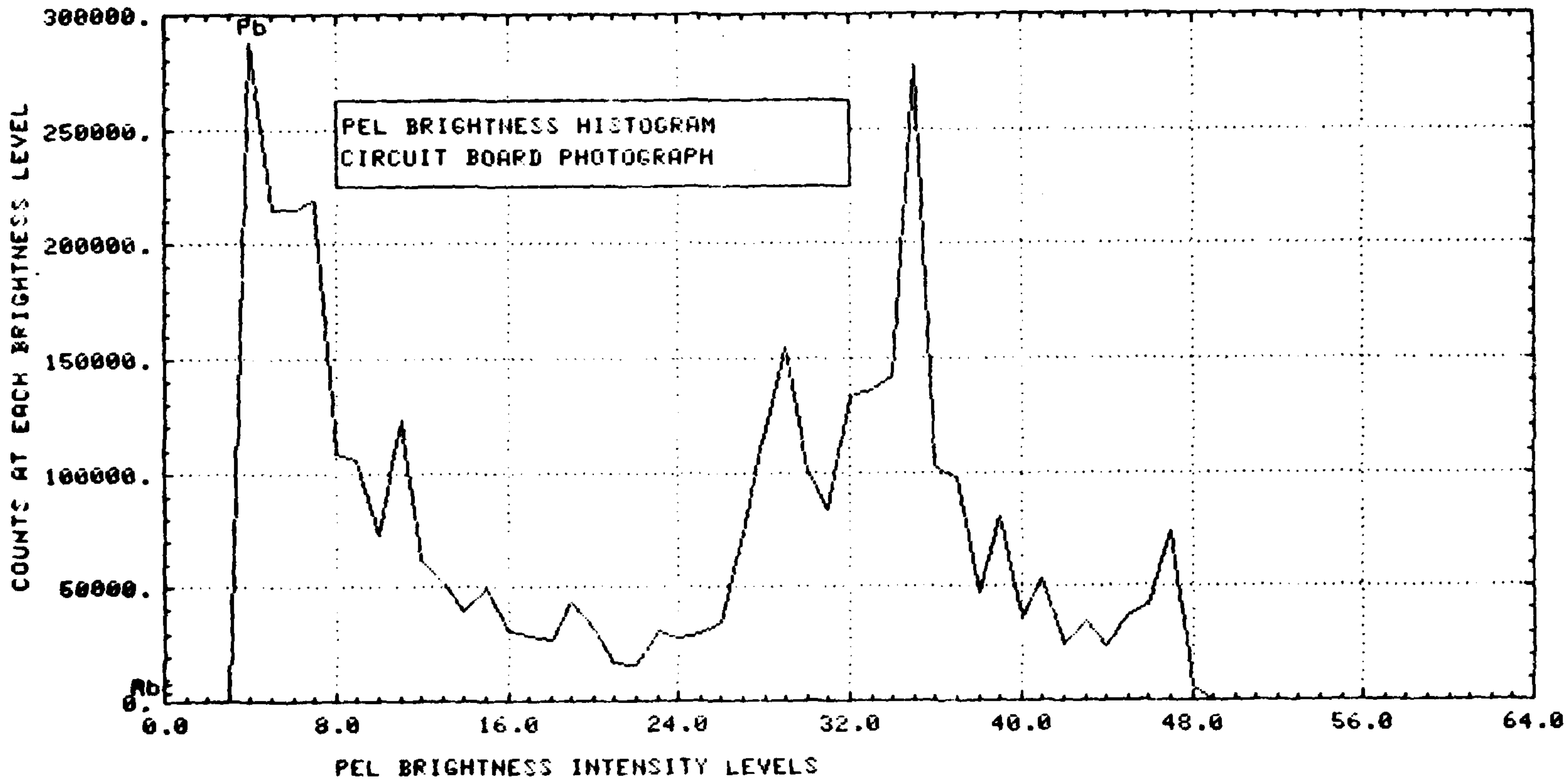


Figure B42b. Linear plot of subject 3 histogram.

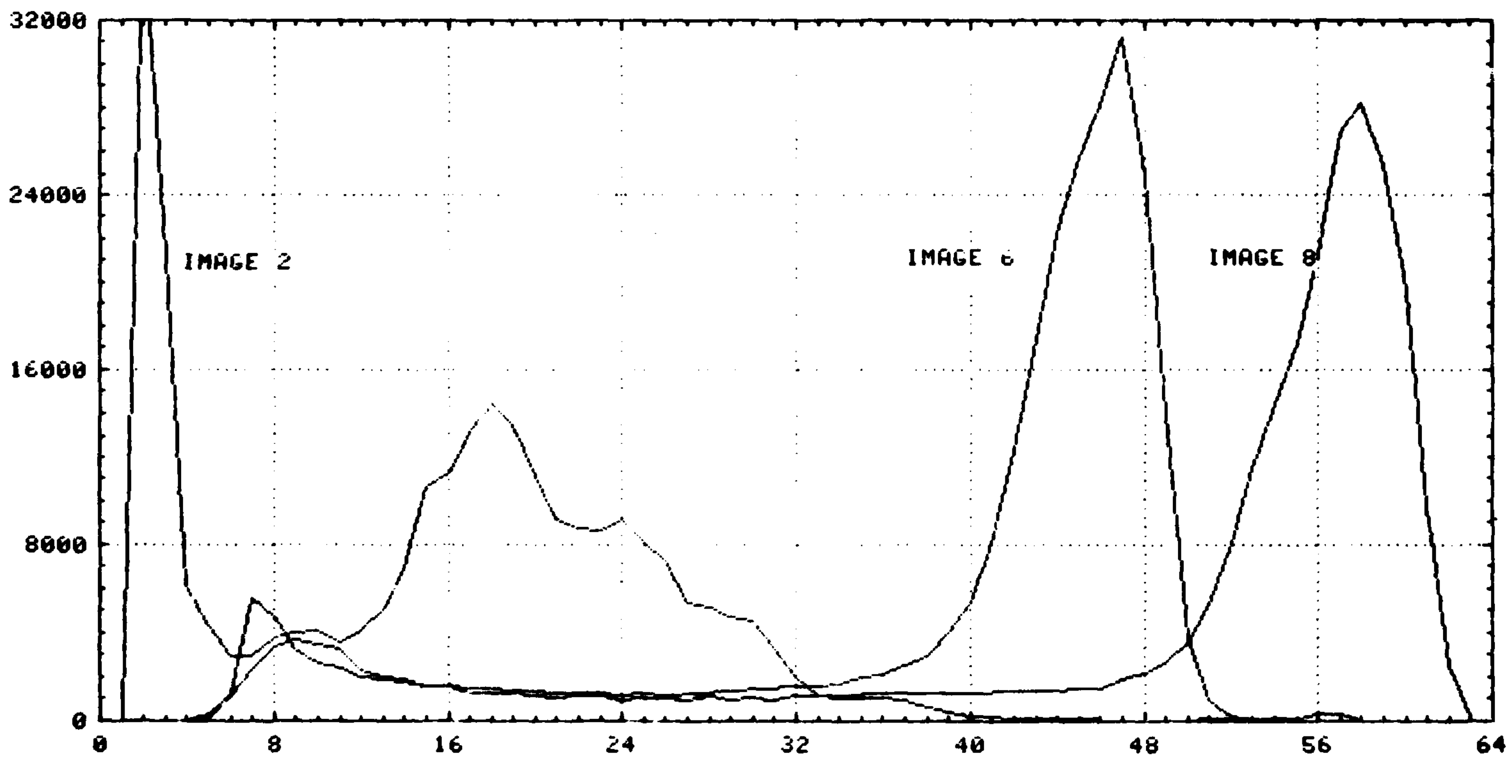


Figure B43. Linear plot of subjects 10, 14, and 16 histograms.

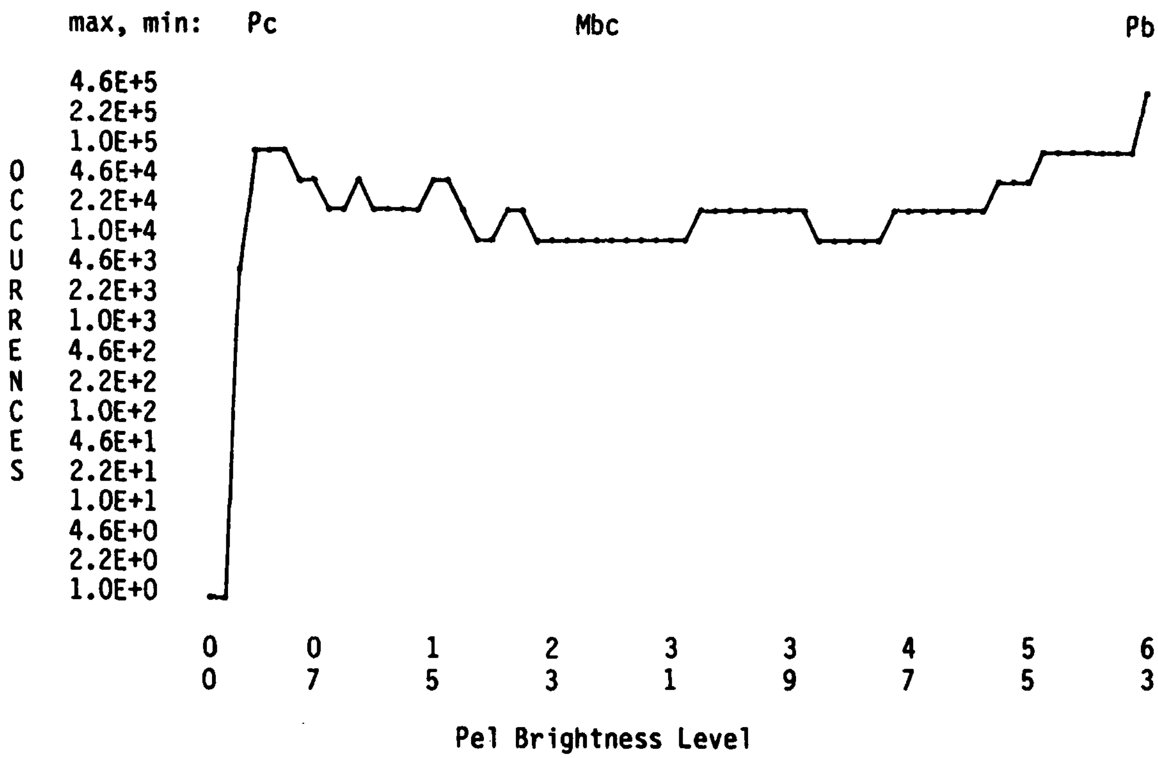


Figure B44a. Semilog plot of sub;ect 4 histogram.

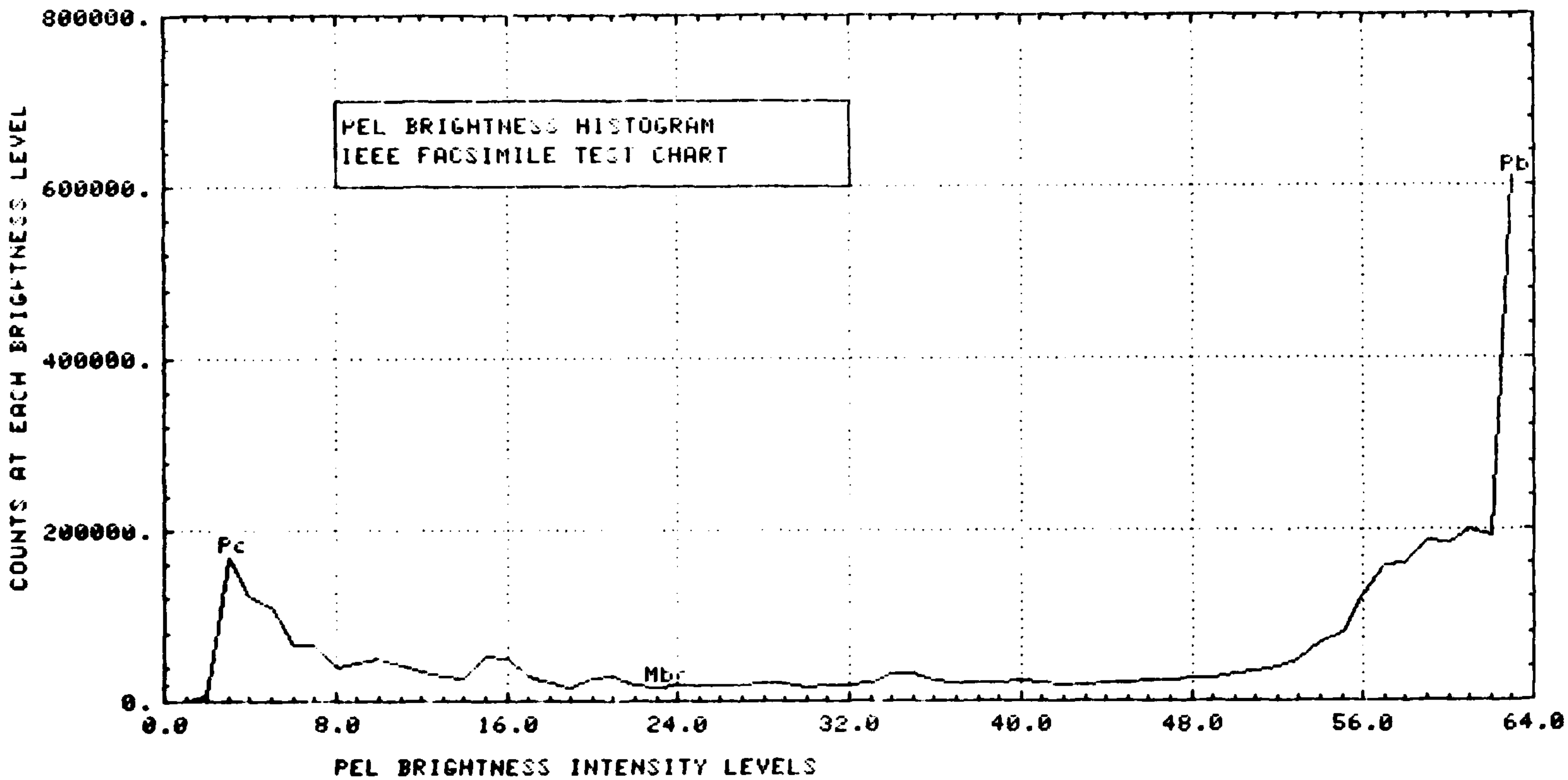


Figure B44b. Linear plot of subject 4 histogram.

SFIv Test 1 (" 2 consecutive partitions exceeded threshold") passed.
8 Partitions exceeded threshold
SFIv Test 2 (" 4 partitions total exceeded threshold") passed.
8 Partitions exceeded threshold

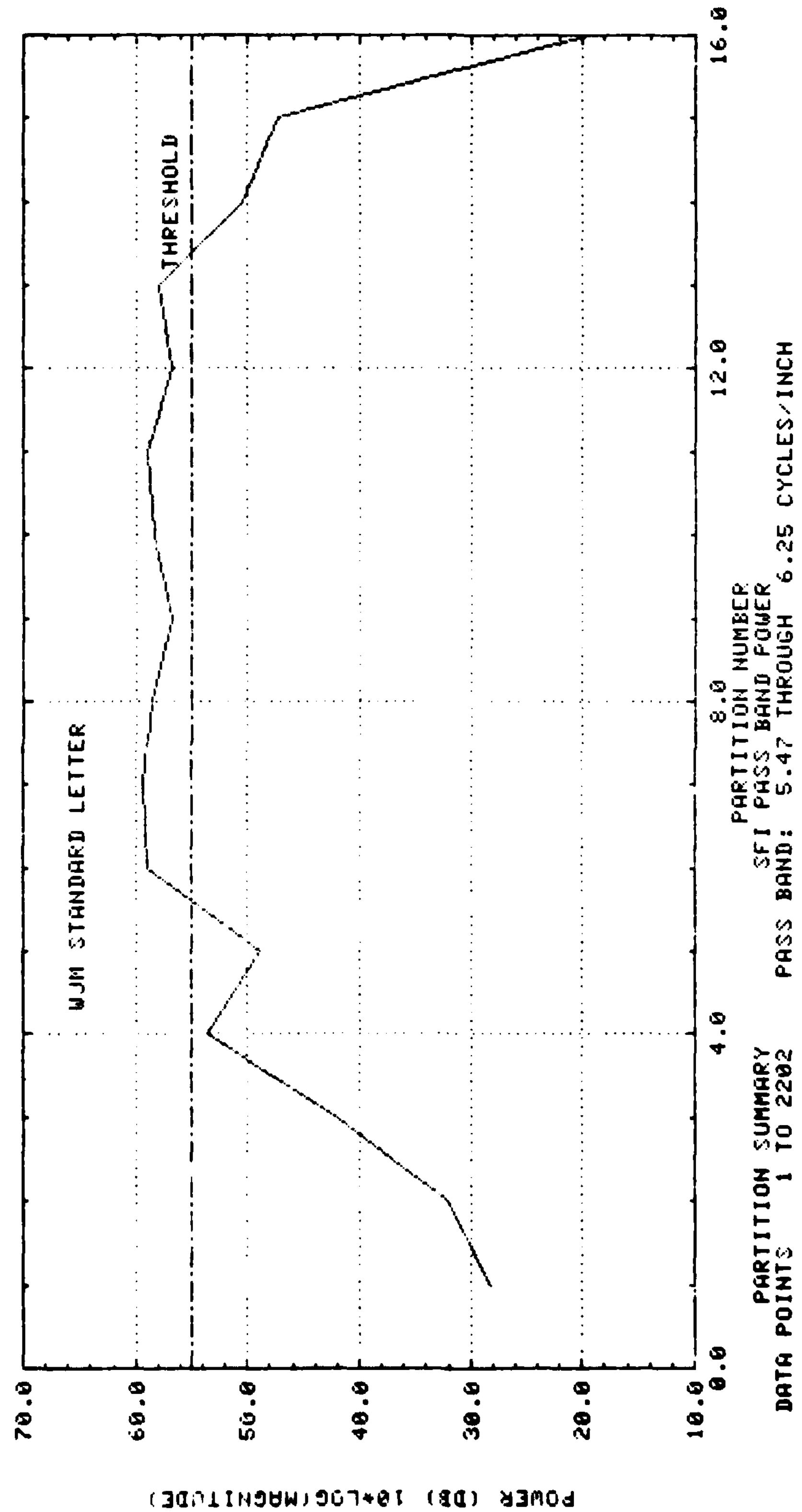


Figure B45. Vertical spatial frequency results for subject 5.

All tests failed, Tests indicate Subject is not all text

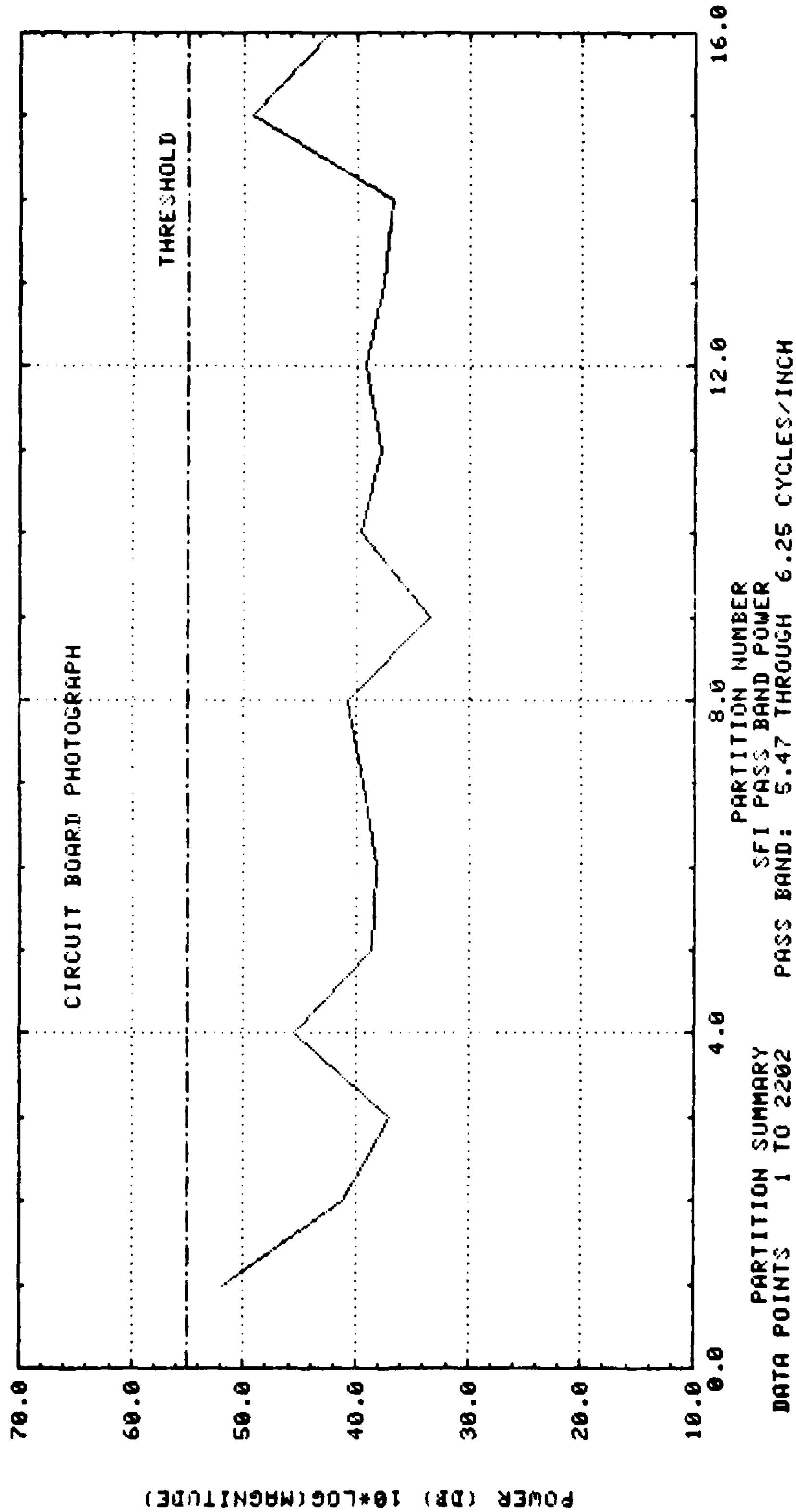


Figure B46. Vertical spatial frequency results for subject 3.

SFIv Test 1 (" 2 consecutive partitions exceeded threshold") passed.
 11   Partitions exceeded threshold
SFIv Test 2 (" 4 partitions total exceeded threshold") passed.
 11   Partitions exceeded threshold

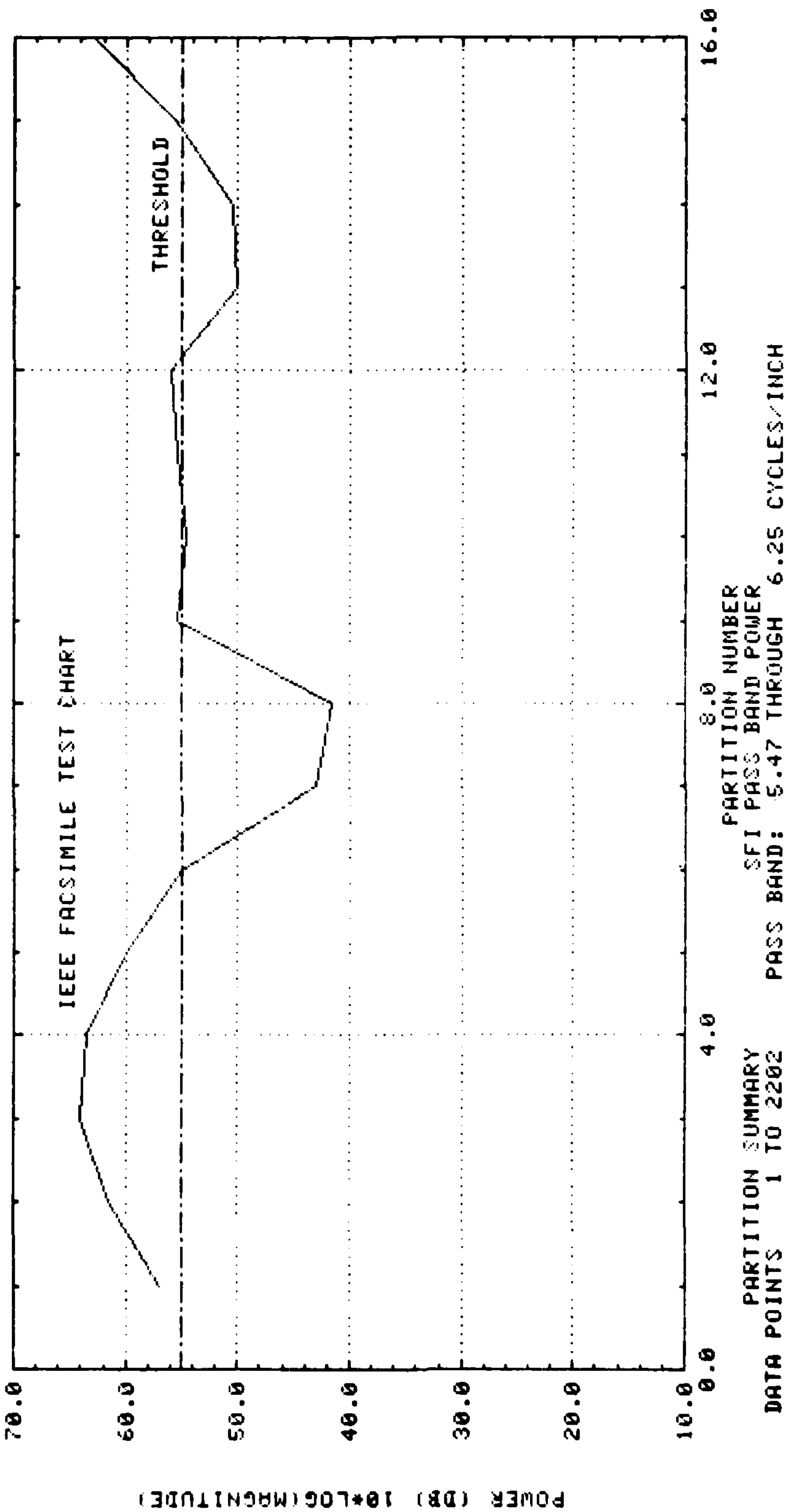


Figure B47. Vertical spatial frequency results for subject 4.

power curve (figure B47). Subject 4 (figure B47) passed both the two consecutive partitions and the four total partitions tests. Therefore, this algorithm needs to be made more restrictive.

The horizontal spatial freauency algorithm has been tested, but less effort has been expended on this than on the other algorithms. Two potential improvements in that algorithm already have been determined. The power threshold should be about 50 dB rather than the 55 dB used for the vertical test. The other improvement is a test for consistency in the power curve. Currently, just one partition need exceed the threshold. The consistency check may need to look for consistency around a straight sloping line because of justified text produced by inexpensive word processors, which add full spaces between words at only one end of the line. Thus, one end of the line may have different spacing from that at the other end.

The results of the algorithm tests are summarized in tables B2 and B3. Table B2 shows the "pass/fail" results of each test, individually. Table B3 shows the bilevel/continuous-tone decision results as based upon the individual test results. Also included in table B3 are the decisions that would be made by a human operator.

Requiring that images be sent by the continuous-tone digitization method unless both the PBS and SFIV tests are passed agrees well with the decision a human operator would make. When it differs, it differs on the side of continuous tone, thus assuring adequate image reconstruction following transmission. So far, each instance of a difference between the human decision and the automatic decision was associated with a preprinted form. In these forms, spatial characteristics differ from standard text. Also, most of the differences occurred when the subject was a small section from a full-page preprinted form. Thus, the first conclusion is that the combination of the pel brightness test and the vertical spatial frequency test appears to be appropriate and sufficient.

The current horizontal spatial frequency test (SFIH) results were compared with the combined test results just mentioned. The SFIH test supported (agreed with) the combined test results only 13 times for 30 subjects (43% support). Ignoring the preprinted form subjects, it supported the combined test results 9 times out of 21 subjects (again 43% support). This SFIH test used the same pass/fail threshold as the SFIV test (55 dB) but required that just one partition exceed the threshold. Unfortunately, such a test accepts subjects that have a strong response in the desired passband over just one partition but rejects subjects that have a more consistent but weaker response. The latter are more likely to be textual. The passband referred to is the one that includes the expected ten to twelve characters per inch. To date, partitions have been chosen to be 156 points, covering a 1.28-inch section of the subject at 200 pels per inch.

As a result of the investigations, an alternate SFIH test is proposed that requires the power of two consecutive partitions and three partitions total to exceed a somewhat lower (50-dB) threshold. The results show this

Subject*	PBS Hist Test	SFIV Test	Current SFIH Test	Proposed SFIH Test
1. Letter	Pass	Pass	Fail	Fail
2. Letter	Pass	Pass	Fail	Pass
3. Circuit bd	Fail	Fail	Fail	Fail
4. FAX	Fail	Pass	Fail	Pass
5. Letter	Pass	Pass	Pass	Pass
6. Letter	Pass--BL	Pass	Pass	Pass
7. Handwritten	Pass	Pass--BL	Fail	Fail
8. Form	Fail--BL	Fail	Fail	Fail
9. Form	Pass	Pass	Fail	Fail
10. Photo	Fail	Fail	Fail	Fail
11. Form	Pass	Pass	Fail	Fail
12. Form	Pass	Pass	Fail	Fail
13. Form	Fail	Pass	Fail	Fail
14. Form	Fail	Pass	Fail	Fail
15. Msg	Pass	Pass	Fail	Fail
16. Form	Fail	Pass	Pass	Fail--BL
17. Cmptr printout	Pass	Fail	Pass	Pass
18. Form	Pass	Pass	Pass	Fail
19. Document	Pass	Pass	Fail	Fail
20. Document	Pass	Pass	Fail	Fail
21. Document	Pass	Pass	Fail	Fail
22. Document	Pass	Pass	Fail	Pass
23. Document	Pass	Pass	Pass	Pass
24. Document	Pass	Pass	Pass	Pass
25. Document	Pass	Pass	Fail	Fail
26. Document	Pass	Pass	Fail	Fail
27. Document	Pass	Pass	Fail	Pass
28. Document	Pass	Pass	Fail	Pass
29. Document	Pass	Pass	Pass	Pass
30. Document	Pass	Pass	Pass	Pass

(The BL suffix indicates a borderline result.)

Note 1. Subjects 9 through 18 contained a 2.56-inch-square portion of the page, the rest using the full page. This means the results have less meaning, since there is no border. The pel brightness ratios may be lower because of the absence of a blank border. The spatial frequency tests were able to consider three partitions only.

Note 2. "PASS" indicates that the document was classified by the test as bilevel; "FAIL" indicates classification as continuous tone.

* Abbreviated title. Full titles are given in table B1.

Table B2. Pass/fail summary of results of classification tests.

	Human Operator		PBS and SFIV Tests		SFIH Test Support			
					Current Test		Proposed Test	
	Bilevel	Cont Tone	Bilevel	Cont Tone	Sprt	Non-Sprt	Sprt	Non-Sprt
1.	X		X			X		X
2.	X		X			X	X	
3.		X		X	X		X	
4.		X		X	X			X
5.	X		X		X		X	
6.	X		X		X		X	
7.	X		X			X		X
8.	X			X	X		X	
9.	X		X			X		X
10.		X		X	X		X	
11.	X		X			X		X
12.	X		X			X		X
13.	X			X	X		X	
14.	X			X	X		X	
15.	X		X			X	X	
16.	X			X		X		X
17.	X			X		X		X
18.	X		X		X			X
19.	X		X			X		X
20.	X		X			X		X
21.	X		X			X		X
22.	X		X			X	X	
23.	X		X		X		X	
24.	X		X		X		X	
25.	X		X			X		X
26.	X		X			X		X
27.	X		X			X	X	
28.	X		X			X	X	
29.	X		X		X		X	
30.	X		X		X		X	
					13	17	16	14

Table B3. Summary of document classification decision results.

test to provide a somewhat higher support of the combined (pel brightness and SFIV) tests. It supported the results 16 times out of 30 (53% support) total and 12 times out of 21 (57% support) for nonpreprinted form subjects. The results are still so scant that there seems to be limited value in this test.

COLOR IMAGERY

The previous investigation into scanning color imagery revealed that much work had to be done to characterize and calibrate the scanner system completely so that repeatable results could be obtained. Further investigations into color separation scanning had been delayed until the CCD 143, its associated circuitry, and the HIC and HEE were completely characterized and repeatable results could be obtained.

Current effort on the TDI imager characterization takes precedence over further investigation into color imagery. Since the CCD 143 and the HIC and HEE are fully operational, however, the color imagery investigation can be restarted following completion of the characterization.

Plans for the next contract period are to resume some testing of the scanner system in order to obtain a set of calibration curves for each of the three color separation passes. These will be tested with a set of color images for both accuracy and repeatability.

CONCLUSIONS FOR APPENDIX B

Initial testing of the CCD 143 imager along with the illumination source and lens combination used on Scanner III has shown that for high quality, multiple-grey-level imagery, there is, at present, an insufficient exposure level for the imager at the rate of 1.5 pages per second. The near-term solution for this problem at NOSC is the use of one of the new lenses in procurement from Alpha Optical, Inc. Tests will be run on the new lens to determine the increase in overall exposure levels on Scanner III as well as resolution capabilities of the lens as compared to the Nikkor lens currently in use.

Testing of the HIC has indicated that it will be a very useful system component, reducing processing time on ICAS by 20-30 minutes for every image captured on the system. The HIC and HEE are also capable of processing both 6-bit and 8-bit images as they are scanned.

Testing of the HEE has demonstrated an interesting problem with the enhancement algorithm. A single pel deviating from its background is not to be enhanced, but all of the closest neighbors of the single pel do get altered. In images that exhibit a small amount of noise or a misalignment of two channels, the edge enhancement algorithm tends to accentuate this noise. This points to a need to align multiple channels of the imager very carefully and/or possibly perform a filtering operation on the image after illumination correction and before edge enhancement. Examples of various filter algorithms have been shown in this report.

Evaluation of the four TRW A/D converters has shown that there are drift problems on the order of 20 millivolts peak-to-peak. This appears to be a slowly varying phenomenon which occurs over several minutes. The accuracy of the A/D converters appears to be +/- 1 LSB, the time-varying drift notwithstanding. Further testing is planned to determine more closely the causes of this drift.

ANNEX A TO APPENDIX B

INVESTIGATION OF NOISE AT THE V_{CC} PIN OF A SCHOTTKY TTL INTEGRATED CIRCUIT

The problem addressed here is noise at the V_{CC} pin (20) of a Schottky TTL octal bus driver, the SN74S244. This noise results from inductance in the V_{CC} power supply system. When a TTL device switches, both transistors of the totem-pole output stage are simultaneously turned on. This generates momentary current spikes in the V_{CC} supply current. Inductance in the V_{CC} supply path then causes noise at the V_{CC} pin of the chip, which in turn is seen at the device output.

An SN74S244 was inserted in a MUPAC 326 universal wire-wrap board with a 0.1 μF ceramic dual in-line package (DIP) capacitor directly above the chip. The input to all eight gates of the 'S244 was a 21-MHz square wave. Outputs were open. All interconnects were made with AWG 30 wire with Milene insulation. Modified wire-wraps were used; these result in about 1-1/2 loops of insulated wire around the wire-wrap pin. The ground pin (10) of the 'S244 and the pin for the adjacent capacitor were wire-wrapped to the nearest board ground pin, with minimum-length wire (see figure BA1). Pin A is the wire-wrap pin into which is inserted one of the two leads of the 0.1-μF capacitor, the other being grounded. Pin C is the nearest board V_{CC} wire-wrap pin. Pin B, corresponds to the V_{CC} pin (20) of the 'S244. Pins A, B, and C were wire-wrapped in various configurations, and measurements of noise at pin 20 and of current between pins C and B were taken as described below.

Case I (Shown in figure BA1). Power is supplied to pin 20 of the 'S244 via a 1-1/2-inch loop of wire between C and B. A current probe is attached to this wire. Peak-to-peak (p-p) noise at pin 20, measured relative to the board ground plane several inches from the 'S244, is 2.4 volts with 200 mA p-p current spikes observed as shown in figure BA2. The maximum instantaneous di/dt is about 10^7 A/s!

Case II Pin A from the capacitor is connected to pin B (pin 20) by using a minimum length of wire (about 0.1 inch). Current spikes on the C to B interconnect are reduced 60 mA p-p. This reflects the current being supplied by the capacitor. (See figure BA3).

Case III The current probe is removed and a 1-1/2-inch loop from C to B is replaced by a minimum length interconnect of about 1/2 inch. Noise at pin 20 of the 'S244 is still high, about 1.0 volt p-p, but it is greatly reduced from the 2.4 volts p-p measured in Case I.

Conclusion: If Schottky parts must be used, make all efforts to reduce V_{CC} supply inductance, particularly in the vicinity of the chip. Use a high-frequency decoupling capacitor to act as a miniature power supply.

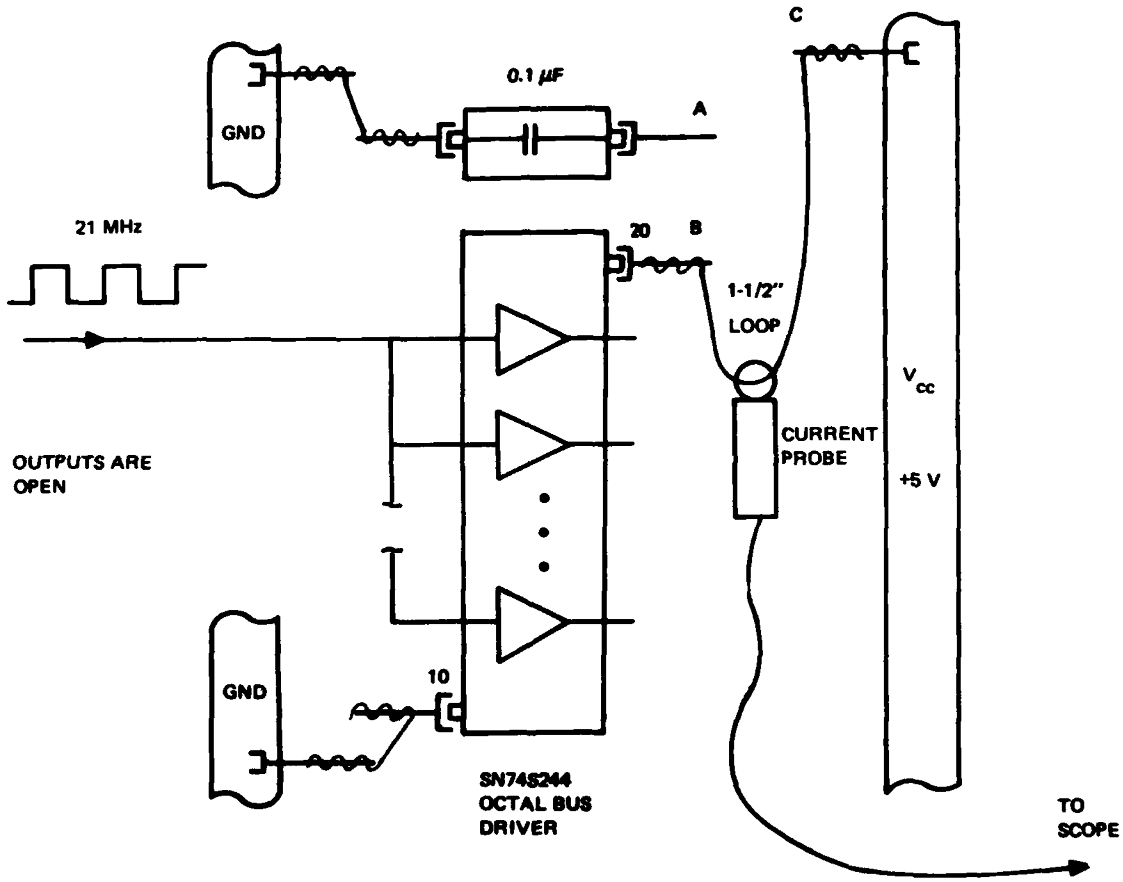
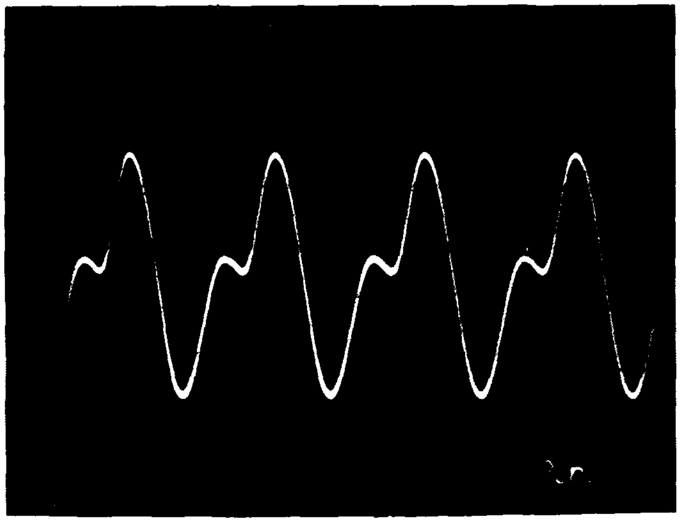


Figure BA1. Test configuration.

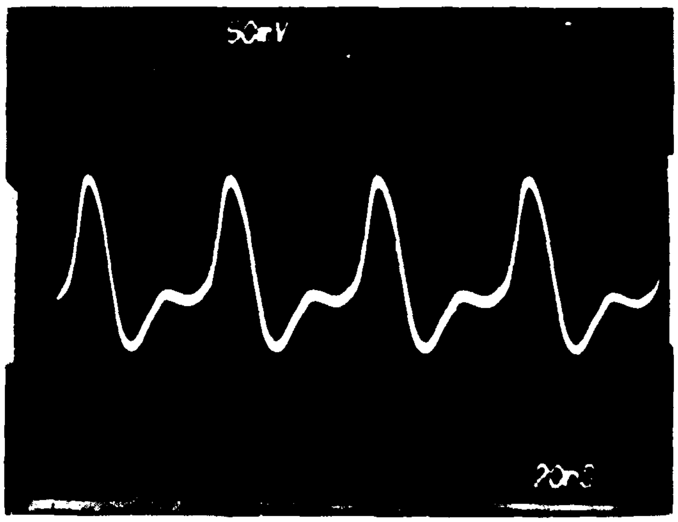
50 mA/div



20 ns/div

Figure BA2. V_{cc} current; case I – no capacitor.

20 mA/div



20 ns/div

Figure BA3. V_{cc} current; case II – with 0.1 μF capacitor.

Locate this capacitor as near as possible to the chip V_{CC} pin and connect it directly to this pin. The other capacitor lead is, of course, grounded. Assuming that a wire-wrap board is used, interconnects should be of minimum length. As can be seen from test results, adding the 0.1 μF capacitor and reducing the length of the C-to-B power wire from 1-1/2 inches to 1/2 inch reduced noise from 2.4 to 1.0 volt at pin 20. The results are summarized in table BA1.

Any distance that the V_{CC} current must travel in the AWG 30 wire-wrap wire is detrimental. For instance, by connecting the capacitor lead A-to-C instead of A-to-B greatly reduces the beneficial effect of the capacitor since current from the capacitor must travel a longer distance to C or to the chip V_{CC} pin.

Use a wire-wrap board such as one of the MUPAC 326 series, whose V_{CC} and ground planes are large in area and relatively thick. In this test, some of the noise generated at the V_{CC} pin (20) was also seen between the V_{CC} and ground planes in the immediate vicinity of the chip. However, because of the board design, this noise was not propagated throughout the board on the V_{CC} and ground planes.

The ultimate solution to these problems is to use a specially designed Schottky wire-wrap board. These are constructed as large capacitors with the V_{CC} and ground planes interlaced and the V_{CC} and ground pin sockets connected directly to these planes. However, most manufacturers of Schottky wire-wrap boards do not yet offer universal pin patterns.

	V_{CC} (pin 20) current spikes p-p (mA)	V_{CC} (pin 20) noise p-p (volts)
Case I: figure BA1 A-to-C 1.5 in	200	2.4
Case II: connect A to B A-to-B 0.2 in	60	
Case III: remove probe minimize C-to-B C-to-B 0.5 in		1.0

Table BA1. Test results summary.

APPENDIX C

DEPARTMENT OF DEFENSE FACSIMILE
DATA COMPRESSION STANDARD WITH
PERFORMANCE COMPARISONS

by

CE Winterbauer

Code 7323

APPENDIC C CONTENTS

APPENDIX C ILLUSTRATIONS

APPENDIX C TABLES

ABSTRACT

A facsimile interoperability data compression standard is being adopted by the US Department of Defense and other North Atlantic Treaty Organization (NATO) countries. This algorithm has been shown to perform quite well in a noisy communication channel. Details of the standard are given as well as comparisons with other data compressions with built-in error protection. This effort was performed under direction of the Naval Electronic Systems Command, PME 110-221.

INTRODUCTION

The Department of Defense (DoD) has a requirement for a ruggedized facsimile unit to be used in a tactical environment. The requirement is being fulfilled by the procurement of a Tactical Digital Facsimile (TDF). Presently the program is moving into procurement of the first production units.

Concurrently, the US is participating in a NATO working group for the purpose of establishing a facsimile interoperability standard for all of the NATO countries. The DoD intends to adopt the NATO standard as the TDF data compression algorithm.

For the NATO standard, the need is to standardize on the signaling protocols and the in-message technique. The requirements pertinent to interoperability are listed in table C1, below.

Operational modes	Acknowledge, negative acknowledge, and broadcast	
Data rates	2400 bps, 16 kbps	
Interface	Digital (CCITT V.24 recommendation)	
Noise conditions		
Signaling	10^{-2} bit error probability	
Message	1×10^{-3} bit error probability and bursty channels	
Resolutions	Horizontal	Vertical
	4.02 pels/mm	3.85 lines/mm
	8.04 pels/mm	3.85 lines/mm
	8.04 pels/mm	7.70 lines/mm
Horizontal Pels	1728	
Scan Width	215 mm	
Scan Direction	Left to right, top to bottom	

Table C1. Interoperability requirements summary.

SIGNALING PROTOCOLS

The signaling protocols consist of the start of message (SOM) and end of message (EOM). These are necessary to provide the receiver with the parameters pertinent to the subsequent transmission and to signal the end of the facsimile transmission. The initial signal must be capable of being successfully transmitted through a 10^{-2} bit error probability communication channel. The protocols must signal the resolution setting, the grey scale setting, the mode of transmission (uncompressed, compressed), and the mode of error correction.

START OF MESSAGE

The SOM utilizes a set of 15-bit pseudorandom number (PN) binary patterns (sequences) in various combinations to signal through a noisy channel and to indicate a set of conditions. Figure C1 indicates the basic concept, and figures C2 and C3 illustrate the details of the signaling code. The "X" interval ranges from one to 52 bits for the command SOM frames. Figure C4 defines the interval value in terms of the command information. This information is sent in the first three SOM command frames and is followed by a second set of SOM forward error correction (FEC) control frames. While three sets of each are sent, only one set of each needs to be detected at the receiver. As indicated in figures C2 and C3, a logical inverted EOM is sent prior to the first SOM frame. With appropriate circuitry, the logical sense of the incoming data can be detected and inverted as necessary. This overcomes the situations in which the communication channel inverts the data. The second set of SOM frames can have an X value of either 254 or 255. When FEC is invoked, the interval is 255. This value added to the total number of bits in the PN sequence gives a value of 315 for each FEC control frame, allowing FEC block synchronization (explained in the section on interleaving).

END OF MESSAGE

The EOM procedure is composed of sixteen S_1 PN codes. The receiver need only detect four in sequence to determine the EOM. This is also illustrated in figures C2 and C3. In these figures, RTC stands for "return to control."

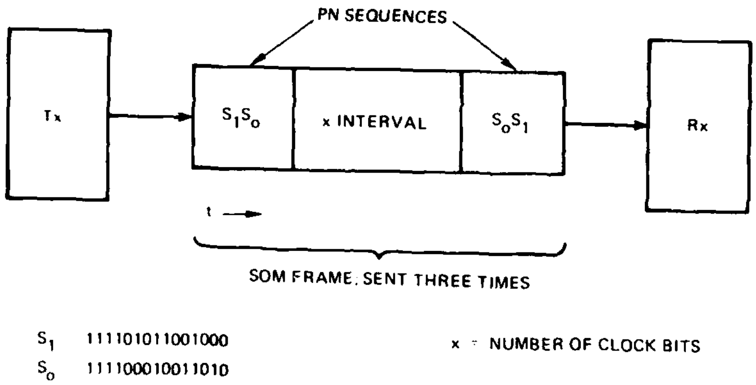


Figure C1. Basic signaling concept.

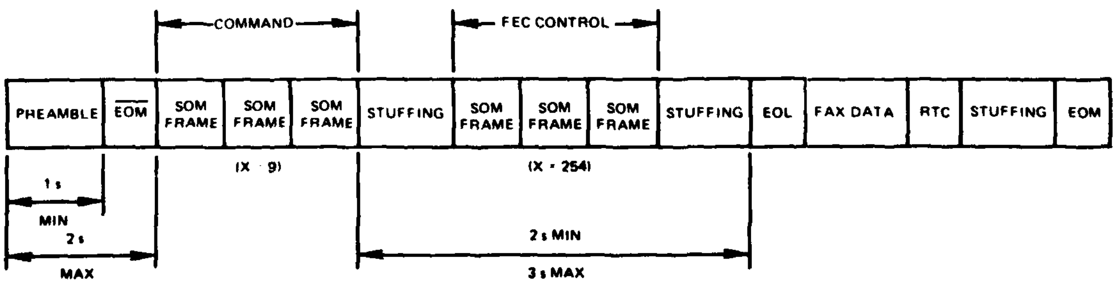


Figure C2. Format without FEC invoked.

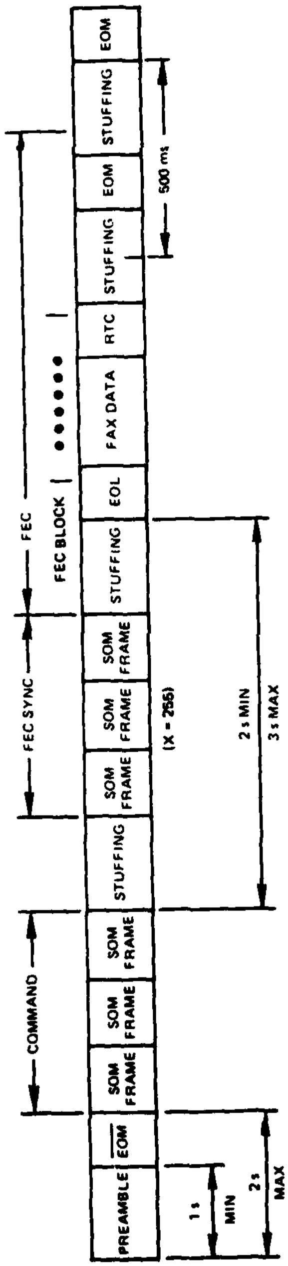


Figure C3. Format with FEC invoked.

SOM FRAME

S_1	S_0	X	S_0	S_1

↑ Represents the number of transmitted bits (all 0s or all 1s) defined as follows:

Number of Clock Periods (X)		Mode Indicated	SOM Type
Compressed	Uncompressed		
1	33	2 GS 3.85 lines/mm feed resoln 4.0 lines/mm scan resoln	
2	34	4 GS 3.85 lines/mm feed resoln 4.0 lines/mm scan resoln	
3	35	8 GS 3.85 lines/mm feed resoln 4.0 lines/mm scan resoln	
4	36	16 GS 3.85 lines/mm feed resoln 4.0 lines/mm scan resoln	
NATO Type I	Interoperability		
9	41	2 GS 3.85 lines/mm feed resoln 8.0 lines/mm scan resoln	
10	42	4 GS 3.85 lines/mm feed resoln 8.0 lines/mm scan resoln	Command
11	43	8 GS 3.85 lines/mm feed resoln 8.0 lines/mm scan resoln	
12	44	16 GS 3.85 lines/mm feed resoln 8.0 lines/mm scan resoln	
17	49	2 GS 7.7 lines/mm feed resoln 8.0 lines/mm scan resoln	
18	50	4 GS 7.7 lines/mm feed resoln 8.0 lines/mm scan resoln	
19	51	8 GS 7.7 lines/mm feed resoln 8.0 lines/mm scan resoln	
20	52	16 GS 7.7 lines/mm feed resoln 8.0 lines/mm scan resoln	
254		FEC not used	FEC Control
255		FEC used	

Figure C4. Detailed X signaling values.

IN-MESSAGE PROCEDURE

The in-message procedure involves the process of encoding the raw facsimile data for inclusion into the data format. The standard allows the facsimile data to be sent uncompressed, compressed without error correction, or compressed with error correction. The uncompressed mode is straightforward where the digital data representing the pel value are directly processed into the data format. The compressed modes with and without FEC are more complex and are explained in more detail. The FEC is utilized for both bilevel and grey scale image data.

FORWARD ERROR CORRECTION

The Bose-Chaudhuri-Hocquenghem (BCH) coding scheme used is summarized in table C2.

Block length	63 bits
Information bits	51
Check bits	12
Error correcting capability	2 bits
Redundancy	23.5%
Generator polynomial	$G = X^{12} + X^{10} + X^8 + X^5 + X^4 + X^3 + 1$

Table C2. BCH parameters.

INTERLEAVING

When the FEC is invoked, an interleaving register is used to distribute burst errors. The register dimensions are 63 by 5 bits (315 bits total). The FEC signaling protocol has an X interval value of 255. Added to the 60 PN sequence synchronization bits of each SOM frame, this yields a sequence of 315 bits. At the receive side of the transmission, the detection of the PN sequences allows proper alignment into the de-interleaving matrix, forcing each 63-bit group in the matrix to be a 63-bit BCH block after the 315 bits of the last SOM frame have been shifted out.

BILEVEL MODE

The data compression technique is the CCITT T4 recommendation for standard-size documents. The oversize document and the corresponding additional codes are not included in the standard.

The exact data format for the bilevel mode is not illustrated. It is simply the modified Huffman code (CCITT T4), selected and placed into the data

stream in the position labeled FAX DATA in either figure C3 or figure C4. The return to control (RTC) is the same as the T4 recommendation, ie six consecutive EOLs. The zero fill is the same as in the T4 recommendation and can also be inserted between lines of data to meet the 20-millisecond minimum line time as stated in the T4 recommendation.

Compression performance. While the decision on the exact type of data compression algorithm was made by committee, the Naval Ocean Systems Center performed many tests to verify, to the satisfaction of the US team, the assertions of the other countries regarding the suitability of the algorithm. Table C3 illustrates the compression ratio (C/R) of several documents. Since the compression scheme is essentially the CCITT T4 technique with FEC overhead, the results indicate only the reduction in compression efficiency due to the extra overhead.

Document	C/R W/FEC	C/R W/O FEC
Overlay	7.1	8.8
Invoice	6.6	8.1
Message form	7.5	9.3
NATO Unclass	6.1	7.5

Table C3. Compression ratios for various documents.

Noise sensitivity. The data compression algorithm is implemented on the Naval Ocean Systems Center UNIVAC 1100/82 computer. For testing purposes, substantial noise data were available from the West Germans and the US Army in the form of digital tapes with actual vhf noise data. These data were injected into the compressed data stream. Four files, which represented the range of noise statistics, were used extensively. The characteristics of these data files are summarized in table C4.

The test document "NATO UNCLASSIFIED" was scanned and subjected to the noise data, both with and without FEC. Figures C5a, C5b, C6a, and C6b illustrate portions of the document with the conditions specified.

GREY-SCALE MODE

The grey-scale mode has the essence of the bilevel technique but differs in several ways. Particularly, it performs some preprocessing prior to run-length encoding of the data. First, the binary data are Gray coded. Second, the data are organized into bit planes. Third, each bit plane of the

Noise File No	No of Burst	Avg Burst Length	Burst Error Rate	Bit Error Rate	Avg Error /Burst
45	2465	5.6	2.6×10^{-3}	8.4×10^{-3}	3.2
46	1768	4.5	1.9×10^{-3}	5.6×10^{-3}	2.9
47	219	4.6	2.3×10^{-4}	6.0×10^{-4}	2.5
55	10 044	1.3	2.1×10^{-3}	2.2×10^{-3}	1.1

Table C4. Noise files utilized for test.

data is grouped into line pairs. Fourth, the line pairs are subjected to a wobbling process followed by a process called autoresolution. Finally, run-length encoding is performed, but the run-length data are encoded by using the black table of the T4 modified Huffman codes. Because of the two-line processing and the limit of 1728 pels per maximum-length run, the line pair is divided into half-line pairs. That is, one half-line pair is processed, a synchronization word is inserted, then the second half-line pair is processed, followed by a second synchronization word.

The format of the in-message data for grey-scale images is shown in figure C-7. The uses of some of the fields are explained in the following text. The terms BILP and BOLP stand for beginning of intermediate line pair and beginning of line pair, respectively.

Gray coding and bit plane processing. Gray coding and bit plane processing are not new techniques. Gray coding causes single grey-level transitions to affect only one bit plane. Bit plane processing simply separates the multiple bits per picture element per line into single bit planes of the line.

Wobble. Figure C8 illustrates the concept of wobble. Wobble is incorporated to take advantage of vertical as well as horizontal redundancy. Under most conditions, greater redundancy reduction is possible when incorporating wobble. In figure C8a, corresponding bit planes from two lines are read into buffers A and B from the scanner. If no other process is involved, improvements can be gained in the run-length encoding by reading out the bits in the square-wave pattern and performing run-length encoding as illustrated in figure C8b.

Autoresolution. In connection with the wobble process, an additional process called autoresolution (A/R) is incorporated into some of the bit planes. Autoresolution acts to increase the compression of data by eliminating data changes in areas of low activity. This is accomplished by performing a check on the number of transitions (1 to 0, 0 to 1) on the

1. This typewritten sheet is accepted by the members as one of the official test sheets to be used for the trial runs.

2. In order to couple the output of a radio transmitter to space or to couple the input of a receiver to space, it is necessary in each case [illegible] or receiving [illegible] may be desc[illegible] used to conve[illegible] high-frequency [illegible] into electromagnetic waves.

3. The mechanism of radiation may be explained quantitatively by means of Maxwell's equations. Upon examining the behavior of the RF current in a wire, it is found that not all or the energy at one end finds its way to the other; some is radiated. See Fig 11.1. The transmission line theory will be used.

Figure C5a. Noise file 45, FEC not invoked.

1. This typewritten sheet is accepted by the members as one of the official test sheets to be used for the trial runs.

2. In order to couple the output of a radio transmitter to space or to couple the input of a receiver to space, it is necessary in each case to use some type of structure capable of radiating electromagnetic waves or receiving them, as the case may be. An antenna is such a structure and may be described as a metallic object, often a wire or a collection of wires, used to convert high-frequency current into electromagnetic waves.

3. The mechanism of radiation may be explained quantitatively by means of Maxwell's equations. Upon examining the behavior of the RF current in a wire, it is found that not all of the energy at one end finds its way to the other; some is radiated. See Fig 11.1. The transmission line theory will be used.

Figure C5b. Noise file 45, FEC invoked.

1. This typewritten sheet [illegible] by the members as one of the official test sheets to be used for the trial runs.

2. In order to couple the output of a radio [illegible] to couple the input of a receiver to space, it is [illegible] to use some type of structure capable of radiating [illegible] waves or receiving them, as the case may be. An antenna [illegible] may be described as a metallic [illegible] used to convert high-frequency current into electromagnetic [illegible]

3. The mechanism of radiation [illegible] means of Maxwell's equations. [illegible] rent in a wire, it is found that not all of the energy at one end finds its way to the other; some is radiated. [illegible] line theory will be used.

Figure C6a. Noise file 55, FEC not invoked.

1. This typewritten sheet is accepted by the members as one of the official test sheets to be used for the trial runs.

2. In order to couple the output of a radio transmitter to space or to couple the input of a receiver to space, it is necessary in each case to use some type of structure capable of radiating electromagnetic waves or receiving them, as the case may be. An antenna is such a structure and may be described as a metallic object, often a wire or a collection of wires, used to convert high-frequency current into electromagnetic waves.

3. The mechanism of radiation may be explained quantitatively by means of Maxwell's equations. Upon examining the behavior of the RF current in a wire, it is found that not all of the energy at one end finds its way to the other; some is radiated. See Fig 11.1. The transmission line theory will be used.

Figure C6b. Noise file 55, FEC invoked.

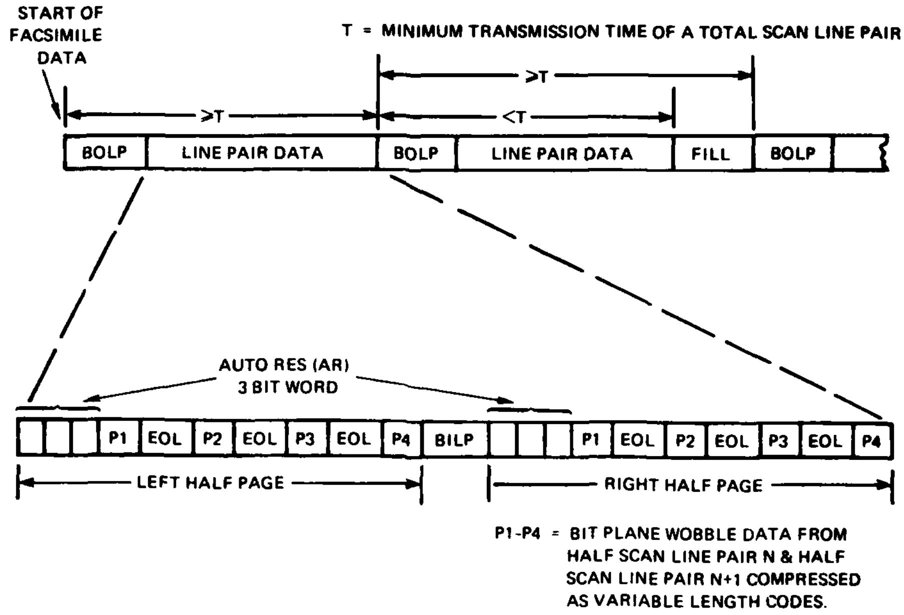


Figure C7. Grey-scale data format.

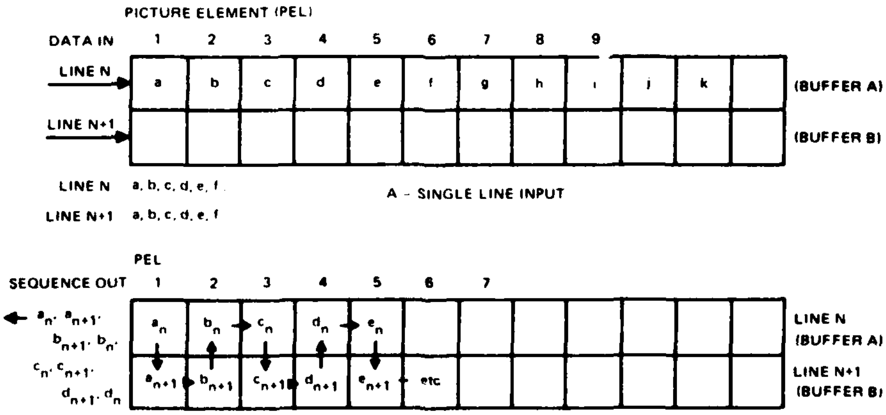


Figure C8. Wobble concept.

wobbled data. If the number of transitions is low (below some threshold), the data are subjected to the autoresolution process. The threshold value has been varied from 20 to 100, and the effects are being evaluated.

To illustrate and explain the A/R process, the wobbled data may be organized into 2 by 2 matrices for the processing. This is shown in figure C9. The data in the 2 by 2 matrices are changed to be all ones or all zeros according to the rules shown in table C5. With those rules used in the process, each 2 by 2 matrix can be replaced with a single bit representing that matrix. These new data are then sent to the run-length encoder and variable-length encoder. The fact that this A/R process took place for that particular segment (bit plane half-line pair) of data is indicated in the format of the data. At the decode side of the process, the autoresolution bit is detected in the format and each bit of that segment is expanded by four after the T4 decoding process. (Note that the original data, shown in step 1 of figure C9, cannot be reconstructed from the decoded/expanded data, so information is lost in this process.) The data are dewobbled, reassembled into the bit planes and individual pels, and then printed.

Autoresolution is not always invoked. The criteria for its use are indicated in figure C10. The 3-bit signaling codes for autoresolution are defined in figure C11. These codes are inserted into the format as illustrated in figure C7.

<u>Modified Huffman table (CCITT T-4 recommendation)</u>. After run lengths are calculated, the data are encoded by using the black code table of the T4 recommendation. In the interest of simplicity, this table is used for both the white and the black runs in the bit planes of the grey-scale data. Other special variations of tables were tried; only small improvements were noted for the four grey-scale images tested.

<u>Compression performance</u>. Four images have been adopted as standards for the NATO working group. These images, referred to as (1) Substation, (2) Microwave Tower, (3) Transports and (4) Ship, are low-contrast reconnaissance photographs. Table C6 summarizes the compression ratios of the four images at sixteen grey levels, with the A/R threshold set at 20.

<u>Noise sensitivity</u>. The four noise files (see table C4) were injected into the compressed data. Figures C12a and C12b illustrate the results of applying two of the noise files against the Substation image.

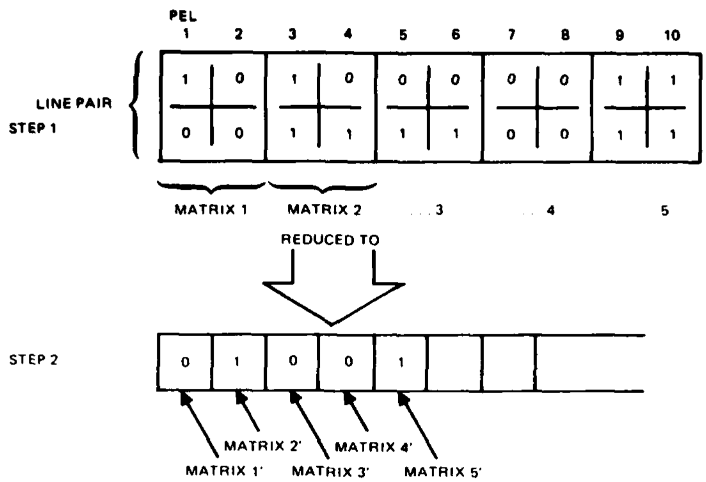


Figure C9. Autoresolution process.

Rule	Number of bits In 2 x 2 Matrix		Transmitted Code	Printed Modified Block
	Zeros	Ones		
1	3	1	0	0000
2	1	3	1	1111
3	2	2	0	0000
4	4	0	0	0000
5	0	4	1	1111

Table C5. Autoresolution matrix rules.

Bit Plane	16 Grey Shades	8 Grey Shades	4 Grey Shades
1 (MSBP)	not invoked	not invoked	not invoked
2	automatic decision	automatic decision	automatic decision
3	automatic decision	automatic decision	discard
4 (LSBP)	low resolution always invoked	discard	discard

Figure C10. Autoresolution/bit plane criteria.

16 Grey Shades		8 Grey Shades		4 Grey Shades	
Code	Meaning	Code	Meaning	Code	Meaning
110	HHHL	110	HHH	-	-
100	HHLL	100	HHL	100	HH
000	HLLL	000	HLL	000	HL

BP1

H = High Resolution
L = Low Resolution

Figure C11. Autoresolution signaling codes.

Image	Without FEC	With FEC
Substation	4.5	3.7
Microwave Tower	6.2	5.0
Transports	4.8	3.8
Ship	4.3	3.5

Table C6. Compression ratios at 16 grey levels.

Figure C12a. Noise file 45, FEC invoked.

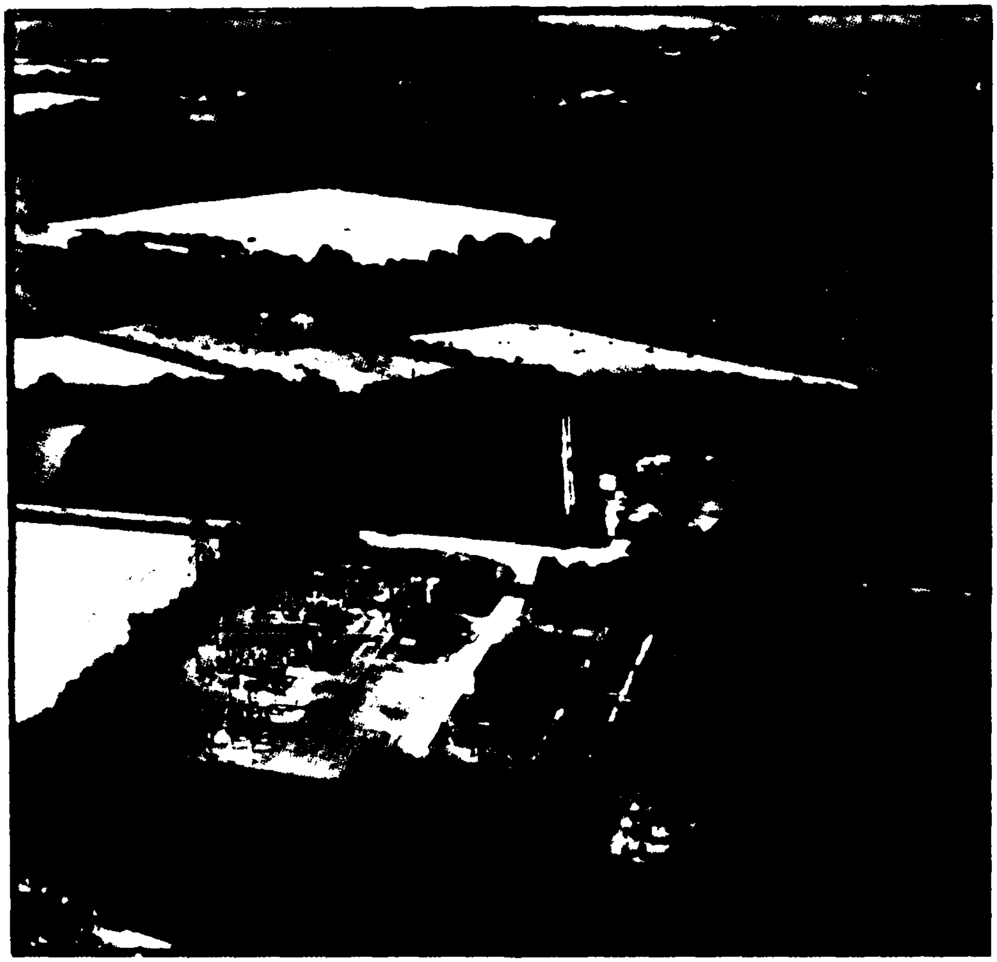


Figure C12b. Noise file 55, FEC invoked.

CONCLUSIONS FOR APPENDIX C

The NATO facsimile data compression standard employs the heart of the CCITT T4 recommendation plus error correction to operate over a noisy communication channel. The error correction is a relatively simple implementation but provides more than adequate protection. Grey-scale capability is added, maintaining the T4 concept without adding extreme complexity.

Unique protocols are employed to provide digital signaling in a noisy channel. The signaling has the capability to indicate the mode of operation and provide FEC synchronization when it is invoked.

APPENDIX D

PRELIMINARY SYSTEM ARCHITECTURE
FOR A
MODULAR REMOTE VIDEO SYSTEM
(MRVS)

by

FC Martin
LA Wise
RW Basinger

Code 7323

APPENDIX D CONTENTS

APPENDIX D ILLUSTRATIONS

SYSTEM OBJECTIVES

The principal objective of the modular remote video system (MRVS) is to provide efficient off-line work stations for a multiplicity of key-entry operators, allowing them to accomplish the sorting process on non-machine-readable letter- and circular-class mail accurately and at a high throughput rate.

INTERFACES

INPUT INTERFACES

The system input interface is made at a flat-bed letter- and circular-class mail belt-type transport system. The transport system separates the mail pieces at 14-inch intervals with dividers. The belt travels at a rate of 84 inches per second. It presents the mail pieces long edge leading, from the bottom of a conventional envelope to the top. The mail pieces may be any thickness from a single sheet to one-fourth inch.

The mail pieces may be torn, bent (lifting the address field up to one inch above the transport belt), smeared, blurred, or dimly legible. The address may be imprinted in colored ink and may be on a colored document substrate or one having low reflectivity, causing the acquired image to have a low print-contrast ratio. The address field may be mixed with an imprinted logo or advertising or may be inside a glassine window. The address field may be in an unconventional location and/or orientation.

The MRVS is adjoined to the belt transport system with an overhead image acquisition system that scans imprinted address information and digitizes, stores, enhances, and distributes the acquired images to the work station displays at a nominal rate of one document per second per operator.

OUTPUT INTERFACES

The output interfaces consist of digital electronic keystroke information resulting from the work station operator's sorting procedures. These signals are made available with MRVS-generated (programmable) delays to activate letter-sorting machine (LSM)-like codes, recirculation-loop input and output control switches, and, as required, demand feeder controls.

SYSTEM PARAMETERS

A number of important system parameters affect the system throughput, error or reject rate, and operator fatigue. Some of these parameters cannot be defined exactly at this time. The MRVS design therefore must be flexible enough to provide the necessary accommodations for variations and minor reconfigurations. The following are some of the principal parameters for the system:

Parameter	Nominal Value	Range
Belt speed	84 inches per second	None--fixed
Document rate	45 per minute (per operator)	None--fixed
Document thickness	Single sheet to 1/4 inch	None--fixed
Document length	12 inches	None--fixed
Document width	12 inches	None--fixed
Number of work stations	Eight per module	None--fixed
Number of modules per system	6 modules	6 to 8 modules
Document scan width	8 inches	5 to 12 inches
Document scan length	8 inches	5 to 12 inches
Document scan density	128 pels per inch	60 to 144 pels per inch
Scanner pel rate	22.5M pels per s	17-30M pels per second
Pel brightness quanta	One bit (facsimile)	3 to 6 bits
Pel array displayed	1024 by 1024 pels	256 x 512 to 1024 x 1024
Display monitor size	11.2 x 11.2 inches	11.2 x 8.4 to 11 x 11 inches
Screen brightness	Operator variable	Fixed at 8-14 foot-lamberts or var
Display phosphor	P-4 white	P-4 white or P-39 green
Display video polarity	Normal (black on white)	Normal or inverted
PBS histogram display contr	Yes	Yes or no
Edge enhancement	Yes	Yes or no

The effects of varying these values will be discussed in the body of the proposed system concept, which follows.

SYSTEM OVERVIEW

An overall system block diagram showing the major system components and indicating data flow is shown as figure D1. Although some variation in equipment component type, location, and performance capability is possible, the general configuration of the system architecture will be as shown.

IMAGE ACQUISITION STATION

The image acquisition system is divided into two major assemblies: the illumination equipment and the scan head.

Illumination Equipment. The illumination equipment consists of a light source with associated reflectors and optics to concentrate a line of light across the conveyor belt in a position superimposed over the scanning area. Several requirements are imposed on the illumination source. First, it must be even in intensity across the entire line to preclude the necessity for using an illumination corrector. Second, its chromatic content must complement the reponse of the charge-coupled device (CCD) imager so that the resulting image acquired has approximately the same appearance as a visual inspection of the same mail piece. For this application a set of two slit-aperture fluorescent lamps is recommended. There exists a difficulty with these (and any other illumination source) to concentrate the light sufficiently. The illumination required for this application encompasses a line 16 inches long by only 0.008 inch in width. The remainder of the light falling on the document is not useful to the sensor and thus contributes only heat and flare, which are two undesirable products in the acquisition process. Intense illumination is required for this application since the document depth of field is large. There is a possibility that four lamps could be used, but there is still the question of whether or not the physical geometry involved will permit a sufficient increase in the total illumination falling on the mail piece to be realized.

Scan head. A lens of aperture no greater than f/4.0 may be needed to satisfy the depth-of-field requirements. A lens having an aperture of f/1.8 would be more desirable, but such a lens has a narrow depth of field. The lens chosen for this application should have a focal length of approximately 85 mm and will be operating at a conjugate ratio of approximately 16 to 1 or less.

The sensor selected for this application is a line-array CCD, the Fairchild CCD 143. This imaging device accommodates 2048 picture elements (pels) and has improved blue spectral response over its predecessor devices.

It is planned that the display work station will present a display of 1024 x 1024 pels representing the image. The scanning device has the capability of acquiring 2048 pels on each line. In the normal operating mode the scan head will transmit the first 1024 pels from each line to the A/D converter. When

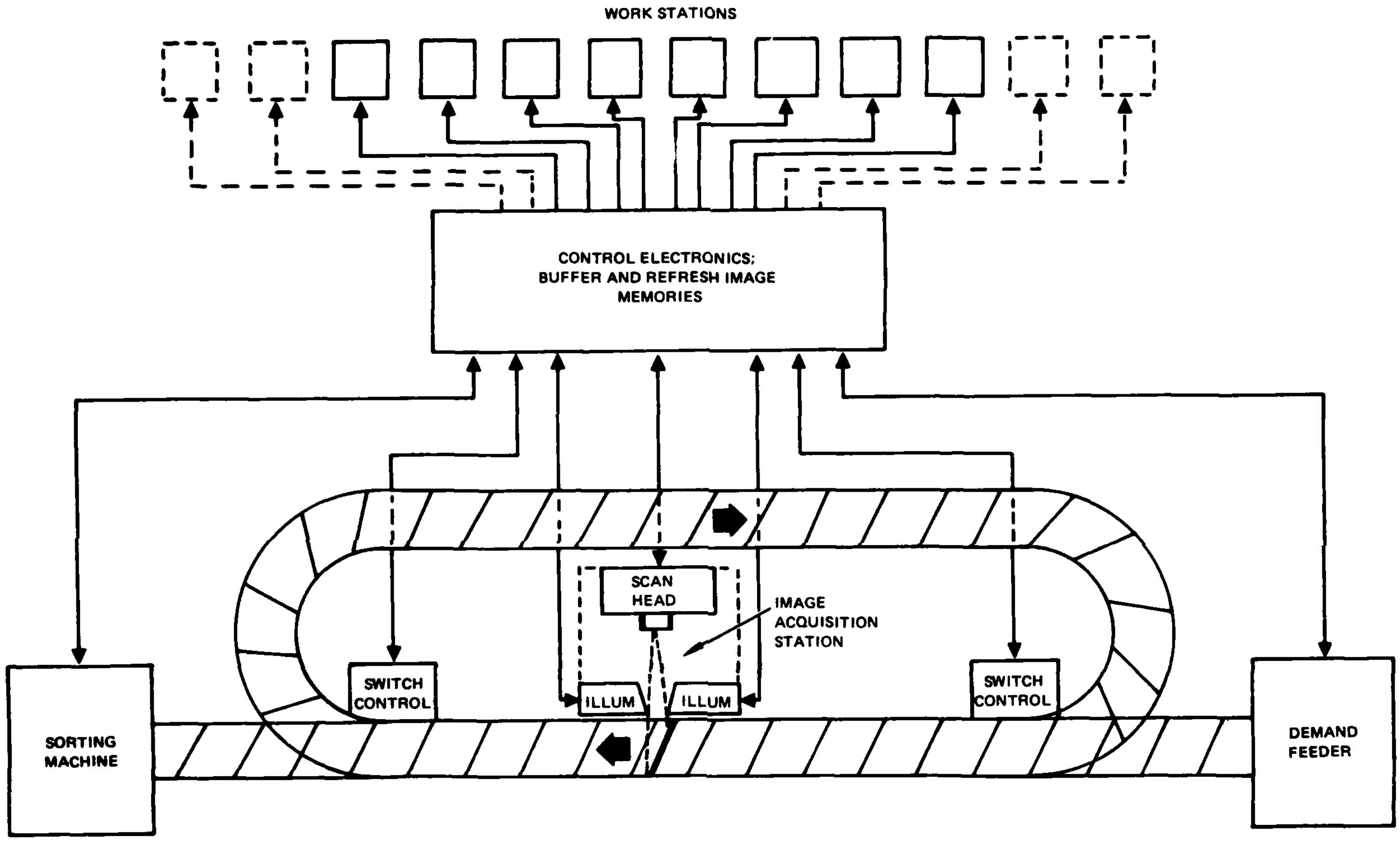


Figure D1. Overall system configuration.

1024 lines are sent, the entire area representing 8 inches by 8 inches will have been acquired. As shown in figure D2, this area encompasses the right-hand edge of the envelope, the bottom of the envelope, and, on a legal-sized mail piece, all except approximately 1-1/2 inches from the left-hand edge.

In cases where the work station operator decides that the total address field is not presented on his display, he has the option of pressing a code (such as "A_1") one, two, or three times, thus incrementing the starting address of the 1024-pel data stream which is sent to the A/D converter to pel position 257, 513, or 769.

By keying such a command, the operator designates the mail piece to be recirculated and rescanned and directs that the scanning area of interest be acquired from an area of the document space shifted 2, 4 or 6 inches to the right of the normal (or default) scan area usually presented. This document can be resubmitted to the same operator or may be assigned to any other operator with the address space properly centered on his work station display.

The scan control electronics does not accommodate the reorientation of address fields that are orthogonal to the normal orientation. This reorientation process will be discussed in the buffer memory section.

ANALOG-TO-DIGITAL CONVERTER

The flow of information through the MRVS is shown in figure D3. Data received from the scan head are presented in analog form to the A/D converter where they are converted to 6-bit digital form. This digital form provides 64 distinct amplitude levels for the pel intensity data. If an 8- by 8-inch scan area is acquired at 125 pels per inch, the incoming data rate is 22.5M pels per second.

The output from the A/D converter module consists of 6-bit parallel words at the rate of 22.5M pels per second. These data are sent to the histogram generator.

HISTOGRAM GENERATOR

Data received from the A/D converter are presented to the pel brightness statistics (PBS) histogram generator for the purpose of accumulating the statistical brightness data pertaining to the scanned image. The histogram generator accumulates a total count of occurrences of each intensity level. Since the image area consists of 1024 by 1024 pels, the total number of pels in the image is 1 048 576, and the sum of all the counts in the histogram will therefore equal this number. If, for example, a page consisted of a uniform reflectivity represented by brightness level 45, there would be 1.048 million samples accumulated in the brightness level 45 register and no others. For images containing principally bilevel (black/white) information,

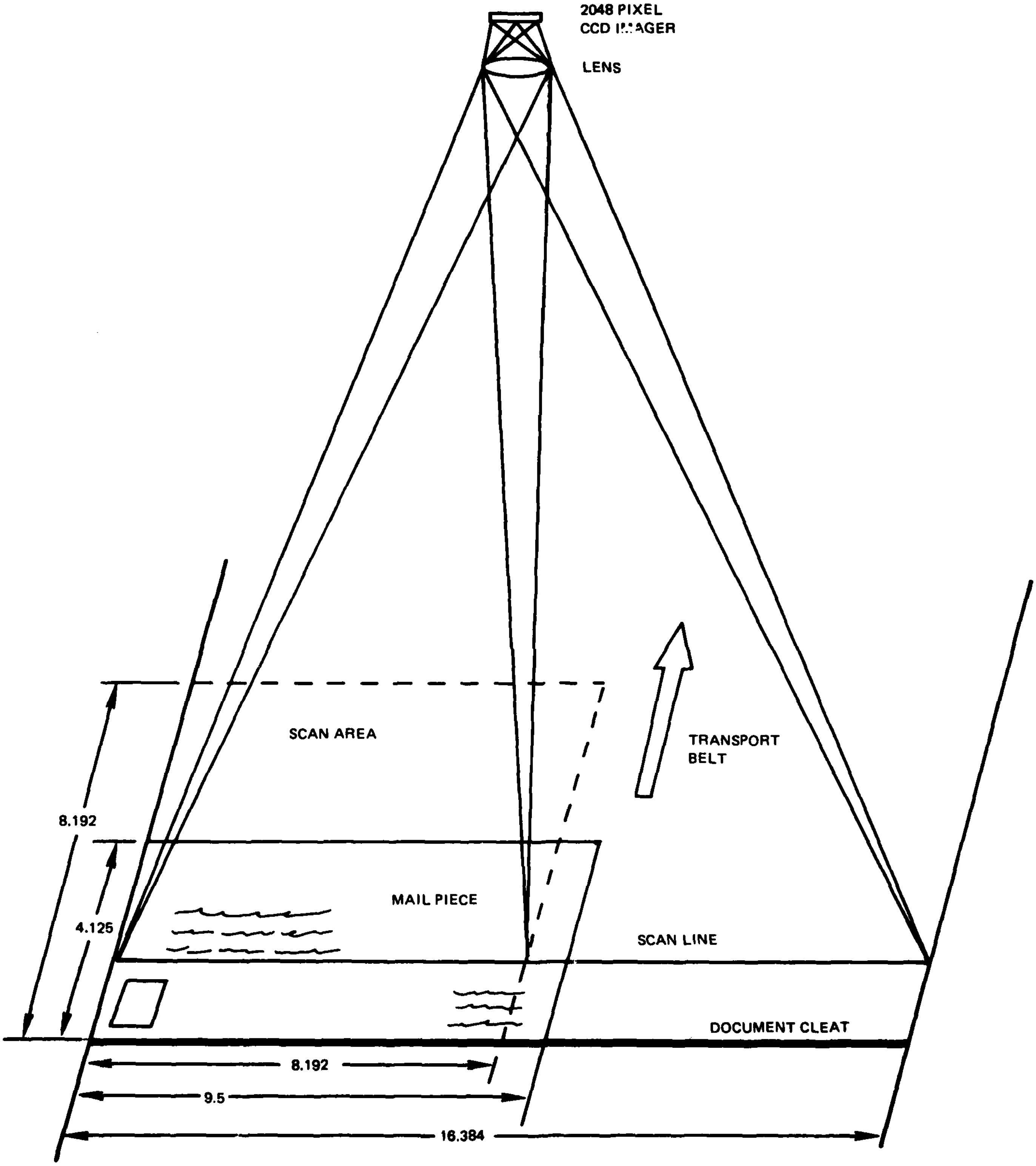
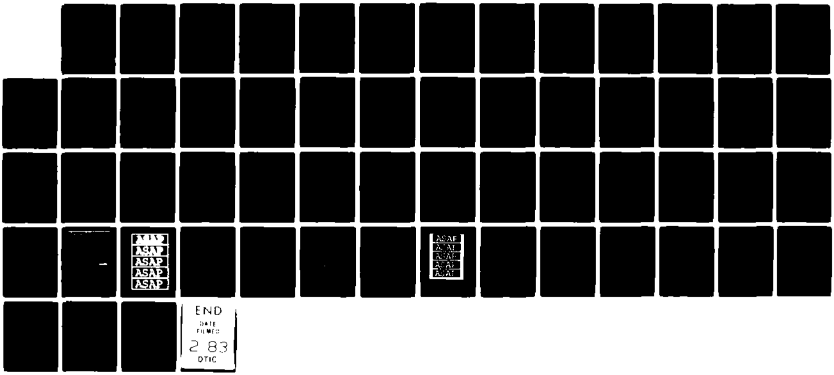


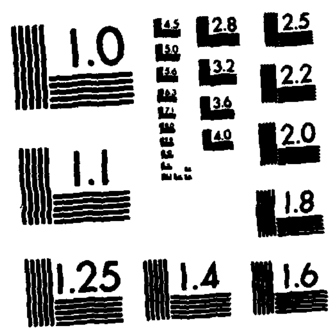
Figure D2. Acquisition station geometry. Dimensions are in inches.

AD-A122 927 ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY EXECUTIVE SUMMARY AND APPENDIXES A-E(U) NAVAL OCEAN SYSTEMS CENTER SAN DIEGO CA MAY 82 NOSC/TR-812

3/3

UNCLASSIFIED F/G 9/2 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

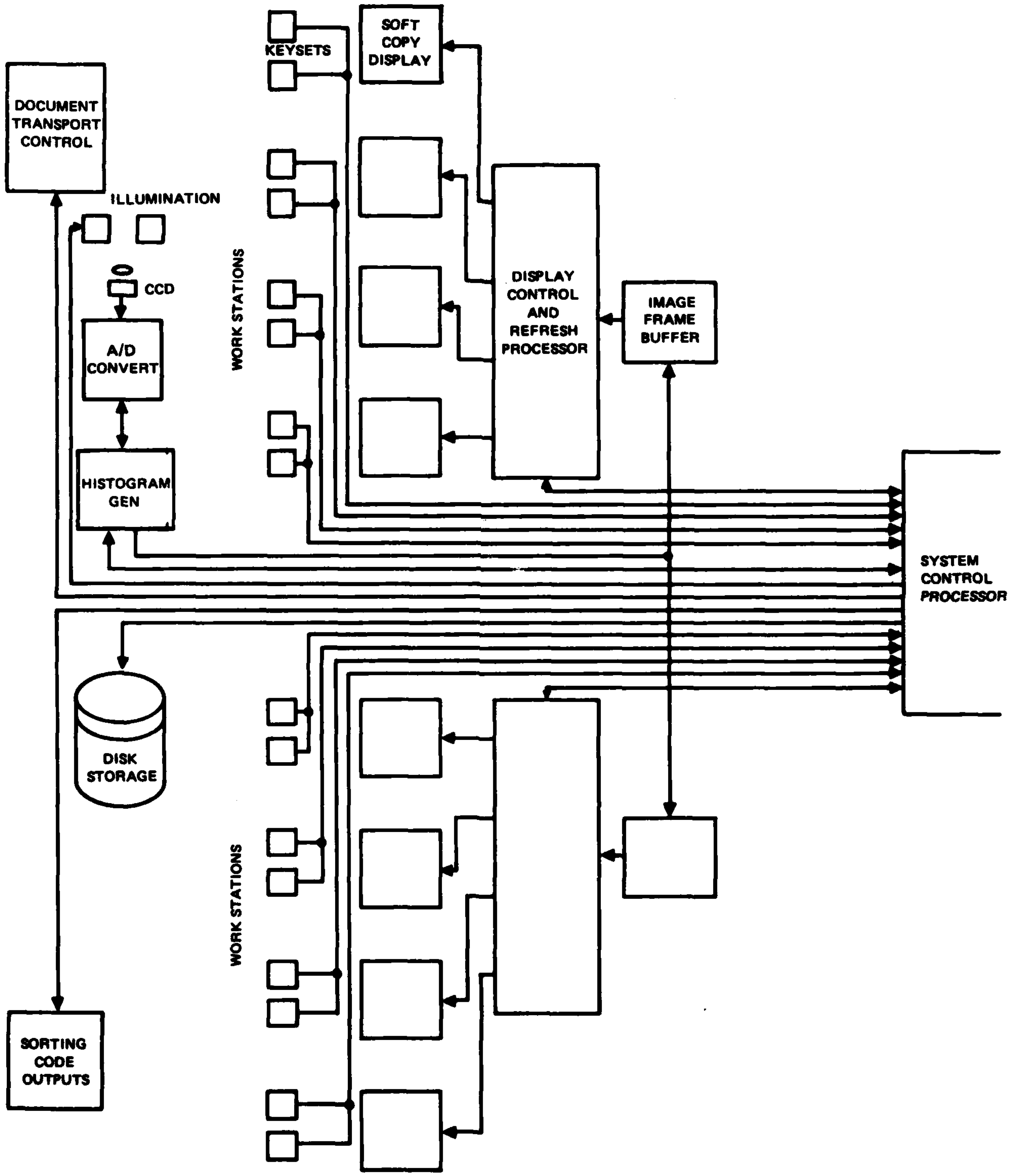


Figure D3. MRVS information flow diagram.

the histogram generally has an appearance of a nonsymmetrical double-humped curve since the image contains principally pels representing the photopic reflectance of the envelope or circular (usually white) substrate. Thus the histogram generator counter receives a preponderance of brighter pel values usually in the neighborhood of brightness level 48. The ink areas are limited to fewer pels having a much lower reflectance. Therefore, the histogram generator also accumulates a smaller sum of pel brightness levels centered around levels 25 to 30. Between these two peaks is a saddle containing pels having intermediate brightness levels generated when pels lie partially on the document substrate and partially on a typewritten or handwritten stroke of an address character.

The purpose of the histogram generator is to establish the upper and lower limits of brightness levels within the image. Using this information, it is possible to threshold the image for transmission and presentation to the work station operator. With clearly written enveloped mail having no advertising on its face, it is a simple process to establish the brightness values of the envelope substrate and of the address characters.

In the presence of glassine windows, advertising, and logos on envelopes, such a dependence on the pel brightness histogram probably will be unsatisfactory. Mail having such irregular features will yield a very high reject rate if bilevel (facsimile) images whose thresholds are based on PBS histogram data alone are presented to the operators. Therefore, it is recommmended that one or more other special function keys be used to allow the operator to tell the scanner controller to shift the threshold several levels up or down and to request that the mail piece be recirculated and scanned again.

IMAGE FRAME BUFFER

The image frame buffer is placed in the pel data path for the purpose of accumulating the scanned and digitized image area components until a complete image is fully composed. As mentioned previously, the pel data are acquired at a rate computed as follows:

$$R_p = S_b \times D_s \times L_s,$$

where

S_b = belt speed, 84 inches per second
D_s = vertical scan density (direction of belt), 125 pels per inch
L_s = CCD imager capacity, 2048 pels per line

Then

$$R_p = 84 \times 125 \times 2048 \text{ pels per second} = 21.5\text{M pels per second.}$$

This approximate value is the burst rate per line and is calculated without overhead time, which will increase the rate by approximately 5%,

yielding a nominal pel rate of 22.5M pels per second. In the primary system configuration shown here, only 1024 pels are stored per line. During the remaining time between lines (approximately 50%) and time between the bottom of one 8-inch document area and the top of the next 8-inch area (6 inches of belt travel) no data are fed to the frame buffer memory. During this idle time several operations can take place. The most complicated operation is "memory corner turning." The requirement for this operation is to rectify address fields that are received from mail pieces having the addresses orthogonal to the normal orientation. The buffer provides the necessary delay, reformatting, and speed synchronization requirements to transmit a full-screen image to the display buffer memory within the display control and refresh processor in one television frame time.

DISPLAY AND REFRESH CONTROL PROCESSOR

The display and refresh control processor (DARCP) is the most complex component of the MRVS. It contains all of the circuitry for storage of the image data and refresh of the multiplicity of displays at the work stations. It accepts commands from the system control processor pertaining to the rate and sequence of distribution of document images to the work station operators, the image intensity parameters, and the formats with which the images are displayed (split screen, flash replace, slide down, slide left, etc). It is doubtful whether an off-the-shelf DARCP that meets all USPS requirements is available from industry at this time. A brief discussion of the required architectural features of the DARCP is given in the following paragraphs.

Image storage. One MRVS module accommodates eight work stations. Each work station display presents a new image to its operator at a controlled programmable rate, nominally one second per image. Refresh memory is required, to support the digital image being displayed. The dimensions of the scanned image area are 8 by 8 inches, and the digital image storage specified by the USPS to produce the high-quality image is 1024 by 1024 pels. In the interest of economy, a design goal is to present the display by using as few levels of grey scale as possible, with brightness and dynamic range carefully set to preserve the fidelity of the address fields. If this could be accomplished with one bit (facsimile), the dimension per image would be 1024 by 1024 pels by one bit. Cursory examinations of images of irregular envelopes, whereby ICAS is used to scan, digitize, correct illumination, selectively filter, edge enhance, threshold, and display, indicate that up to 4-bit data may be required to produce adequate images.

To accommodate two such images for input buffering and dual or sliding display presentations, the memory requirement for each work station will be two 1024 by 1024 by 4-bit memories. To present flickerfree displays at a 30-Hz frame rate, the display pel rate fed to the DARCP digital-to-analog (D/A) converter is 43M pels per second per display. If the image frame buffer is designed to transfer images into the DARCP with minimum interrupt time, the input pel rate must also be 43M pels per second.

The image frame buffer may be integrated architecturally within the DARCP if it can be designed to perform the high-speed corner turning and

asynchronous buffer loading described above. In any case it should be designed and fabricated to use the same memory modules and data flow strategy so that maintenance and logistic support for sparing are simplified.

If 4-bit images are required, the total memory complement in the DARCP for each of the eight work stations will be sixty-four 1024 by 1024 bit-plane modules, not including the image frame buffer.

Interfaces to the system control processor. In addition to the image buffer port, the input to the DARCP consists of a series of commands from the system control processor. They include

Image buffer transfer requests
Work station image assignment sequences
Image histogram values
Requests for mode and timing of display changes

The DARCP transmits data to the system control processor indicating its status with respect to numbers of available image memories. It also reports to the control processor on results of internal diagnostic tests within the DARCP.

Refresh outputs. Outputs from the DARCP to each of the display monitors consist of eight 4-bit word-parallel output channels. They are connected to eight work station D/A converters, which may be located within the DARCP if the cable lengths to the display monitors are reasonably short (eg, 30 ft). For greater cable lengths, the four data bits, a clock signal, and a sync signal must be sent via six parallel coaxial cables to the A/D converters, which must be located near the display monitors. For long runs, the coax must be selected for low dispersion and low attenuation of the high-frequency components of the pel brightness words. For maximum flexibility of operational modes, the DARCP must accommodate asynchronous and independent rates of changes of image data to each work station. The system must be operable with anywhere from one to eight operators, with a corresponding increase in the document feed rate.

As mentioned previously, there is very low probability of locating manufacturers of equipments whose specified characteristics exactly match the USPS requirements. In a later section of this appendix is discussed an alternative near-term architecture consisting of accessible off-the-shelf component equipments having great flexibility for the evaluation of system throughput as a function of controlled work station parameters. Also discussed later is a proposed development system that can be used to perform alternative system design tradeoffs in the areas of display format, operator interaction, keyset design, etc.

SYSTEM CONTROL PROCESSOR

For several reasons, the primary candidate for the control processor for MRVS is the Digital Equipment Corporation (DEC) PDP-11/34A minicomputer. DEC equipment is easily reconfigurable, meaning that as system requirements change

the system can be modified accordingly. The PDP-11/34A is a medium-capability minicomputer. If the evolving detailed system design requirements dictate that more computational power is needed, then the CPU can be upgraded to a PDP-11/70 or possibly a VAX-11/750. Software already generated would be easily transportable from one system to another. All hardware interfaces would remain virtually unchanged.

The proposed CPU system configuration consists of a PDP-11/34A CPU; an LA120 printing terminal used for system control, software upgrades, and system diagnostics; dual RL02 removable-cartridge 10.4-megabyte disks for system software, operational statistics, training software, and sample images; one or more VT100 CRT terminals for use in operator training; and eight special-design keysets for operator entry.

For MRVS on-line processing, the various tasks that the CPU must perform are outlined as follows.

Demand feed control. If a recirculating transport mechanism is utilized, there must be a demand feed control to allow recirculated mail to be merged into the main delay path to be rescanned. The computer must track each mail piece as it progresses around the delay loop, inhibit the demand feeder at the appropriate time, allow the recirculated mail piece to merge, and restart the demand feeder.

Mail piece tracking. The CPU must keep track of each mail piece as it progresses through the system. There must be means for keeping track of belt speed or at least keeping track of each cleat as it passes a reference detector. The CPU must then update the position of each mail piece every 167 ms on the average. The detector input to the CPU must be on a high-priority interrupt line to initiate this operation.

Threshold control. As each mail piece is scanned, the pel brightness statistics (PBS) will be computed for the digitized image. At the same time, a 6-bit image will be stored in a buffer memory. After the image is scanned, the PBS will be analyzed by the CPU and a threshold will be set in the output control circuitry of the buffer memory before transmission of the image to the display controller.

Display system control. The CPU must control the display system so that the next image is routed to the next available operator. The details of how this is done depend upon the specific system configuration. One possible configuration consists of two standard DeAnza IP8500 display systems, each of which can provide refreshed 1024 by 1024 pel displays for four operators. Each IP8500 would contain four image memories. The CPU would then route the next image to the IP8500 with the fewest images waiting for processing.

The CPU must also control the selection of an image (or images if a split-screen display is used) for display to an operator. After the operator makes the necessary keystroke entry or after a specific time interval, the CPU would then route the next image in the sequence (if one is available) to that operator.

Keyset input. The CPU receives keystroke information as inputs, from each of the eight operators. The exact format depends on the type of sorting being done at a given time. The eight keysets would be implemented by using a priority interrupt scheme so that no keystrokes are missed. The software also would perform error checking on the data input; in case of an obvious error the mail piece would be recirculated.

The CPU must keep the input information matched with the mail piece at all times so that the information can be output to the mail sorting system as each mail piece arrives.

Recirculate gate control. For those mail pieces not fully operated upon for any of a number of reasons, the CPU must control a recirculate gate to allow the particular mail piece to be rescanned and operated upon again. Possible reasons for failure to operate upon the image are lack of operator response, image not legible, address information not in the field of view, address information orthogonal to field of view, etc.

It is recommended that additional function keys be implemented to allow the operator to direct the scanning station to modify its scanning parameters on the next pass through the scanning station. Examples of parameters to be modified are left/right, up/down, orthogonal scan, raise/lower threshold, etc. This would allow eventual processing of many mail pieces that would otherwise be rejected. The CPU would keep track of the scanner commands as well as the number of times a particular mail piece was recirculated, so that the piece could be rejected automatically after some set number of retries.

Operational statistics. The CPU can also record various operational statistics, which might include the number of mail pieces processed (by module, by operator, etc), error rates, and reject rates.

HUMAN ENGINEERING CONSIDERATIONS

The throughput rate of the MRVS is directly related to the efficiency of the operator/machine interface. The major goal of the system is to provide an efficient and comfortable environment for a multiplicity of operators. By the very nature of the task, the operators are placed in a situation of reasonably high stress. They are required to concentrate with almost undivided attention to the work station display, to interpret selected data in the address fields, to make sorting scheme decisions, and to enter keystroke information at a nominal 1-second repetitive rate for an operator shift of reasonable duration. The operators also have knowledge that their individual performance is monitored for quantity and accuracy and is logged for later reference.

Operator environment. Electronic document scanning affords the opportunity for the system designer to isolate the operators from the environment of the transport belt and scanning stations. The practical distance from the scanning station to the work station complex is limited to

approximately 100 metres. Beyond that the engineering problems and cost of transmitting the high-bandwidth image data reliably begin to escalate rapidly.

A key to efficient work stations is simplicity. For this application, the work station is envisioned as a small area isolated to some extent from adjacent operators by movable 6-foot soft sound-deadening partitions. A work station table having a 28-inch surface height, a 25-inch knee height, and a 24-inch knee width is needed to support the display and keysets. The keysets should be movable and be fitted with nonskid feet so that the operators can orient them in a comfortable location for individual preference.

Electronic equipments emitting high noise levels from blowers or rotating machinery must be placed at a remote distance from the operators. Climatic controls such as elimination of drafts, elimination of thermal radiation from sunlit walls, and maintenance of an acceptable even temperature are important. Equipments that exhaust appreciable heat loads must be remotely located to simplify control of ambient temperature in the work spaces. A work station operator may require individual control of his work station environment illumination. A "bullet type" overhead spotlight, controllable by an operator dimmer switch, may provide the most pleasing background for his display environment.

A selection of cassette or live stereo music channels, available from plug-in headphones, might be offered to operators if it can be shown that productivity is not adversely affected.

Display engineering parameters. The most important interface between MRVS and the operators is the soft-copy display. Clarity, contrast, color, format, stability, size, location, and ambient illumination all affect the operator's ability to accurately interpret the data, which are presented at high rates.

An initial parameter to be selected is the field of view presented to the operator. A small field of view limits the ability of the operator to search for detail and confines his area of interest to a "tunnel vision" perimeter. A 12-degree-diameter field of view is considered too small since this solid angle restriction fails to make use of the eyes' agility to scan rapidly. To overcome this limitation, the system would have to provide a cumbersome zooming and scrolling feature to make it possible to examine wider areas of the acquired image. A 60-degree-diameter field of view is considered too large, since the observer must turn his head to examine the periphery of the display area. The resolution of the eye falls off rapidly as a function of angular distance from the center of fixation, so that details are not resolved well in peripheral areas. A 60 degree-diameter field of view also wastes digital image refresh storage resources.

For the MRVS application a field of view of 40 degrees has been selected. As a result of this decision, additional display parameters can be calculated. Figure D4 shows the geometry of the display viewing area with respect to the observer's eye. Given a 15-inch display screen, the resulting

inscribed square image area is approximately 8 by 8 inches. Larger displays, such as a 17-inch monitor, will produce larger images, but should be viewed at a greater distance to keep the viewing angle constant. Unless superior images are produced from the larger display screens due to relatively smaller spot size or better focus, there is no advantage to the larger monitor for single viewer presentations. The 8 by 8 inch dimensions are the same as the acquired scan data area, producing a 1:1 (life size) soft-copy version of the image. The diagonal of the square display is 11.31 inches. The distance, d, between the screen and the viewer's eye that subtends a 40-degree angle across the diagonal can be calculated as 15.34 inches.

Once this dimension is established, it is possible to calculate the angle subtended between two pels on the display screen. Since the 8-inch horizontal and vertical dimensions of the display area are represented by 1024 pels each, the spatial resolution on the soft-copy display is 128 pels per inch. The distance between two pel centers is therefore 0.00781 inches. The angle subtended between these two centers at the viewing distance of 15.34 inches is 0.0288 degree or 1.728 minutes of arc. Since the limit of visual acuity is about 1 minute of arc, the operator should be able to distinguish pels in the center 10 degrees of his foveal vision. This is almost an ideal geometry for the work station display.

Refresh rate for the display is 30 frames per second. This rate is rather low, and some flicker will be noticeable on some display patterns if short-persistence P-4 phosphors are used. This effect will be particularly pronounced with high-contrast patterns of fine detail. A 2:1 interlace will provide 60 fields per second and will somewhat alleviate the flicker problem. A medium-persistence phosphor eliminates the problem but in so doing limits the use of dynamic displays. Medium-persistence phosphors are not available in white.

<u>Information display formats</u>. Unless a subsequent evaluation indicates otherwise, the recommended display for this application is a 1024- by 1024-pel, 30-frame, 60-field, 2:1 interlace format using P-4 white short-persistence phosphor.

If dynamic displays (those showing image motion) are to be used, the image sequences must (or at least should) be synchronized to fields and frames. At a one-document-per-second rate, there are 60 fields with which to present dynamic motion for 1 second.

Some typical formats that might be presented are as follows:

Flash: One new image replacing its predecessor each second.

Shift left: One image "sliding" in from the left and stopping in the field of view for most of the display period.

Shift down: One image "sliding" in from the top and stopping in the field of view for most of the display period.

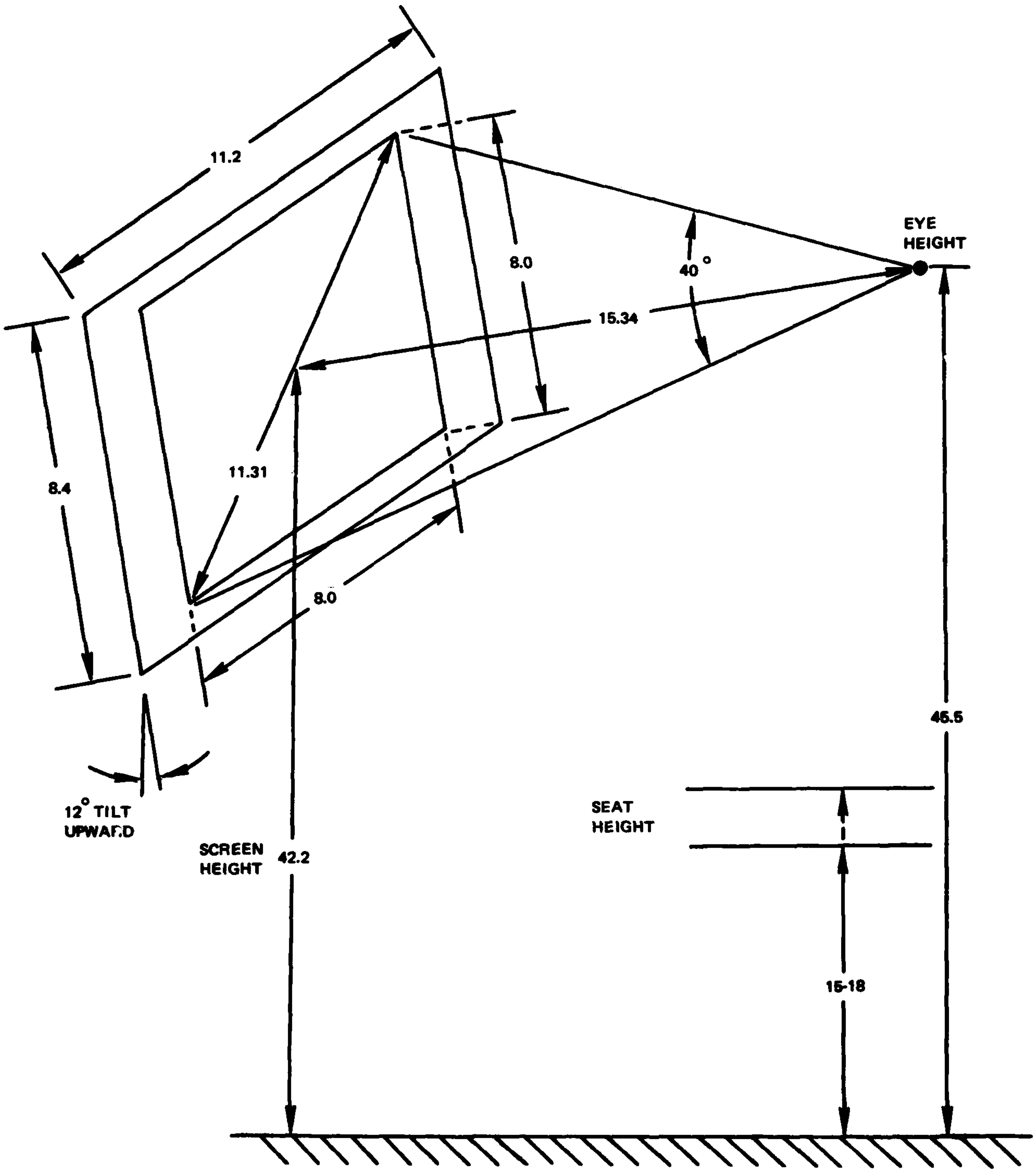


Figure D4. Display viewing area geometry. Dimensions are in inches.

Alternate image: Screen divided, top & bottom; new images alternating between top & bottom.

Other: Lap dissolves, fade-to-black, etc.

Flash replacement of previous document images merely requires the programming of 60 fields of the same image. On the 61st field, the next image is selected for presentation through field 120, etc. The images probably should be presented in normal mode (black on white), with the background (white) level kept as constant as possible.

In the modes that use dynamic displays, two types of motion can be used: continuous and intermittent. With continuous motion, the 1024-pel width or height is divided into 60 equal (as equal as possible) increments of 17 pels each.

For shift-left presentations of one second each, the calculations are easily derived. At each odd field time the contents of the odd field are shifted left by 34 pels. The even field is presented 17 pels to the left of the first odd field. At each subsequent display of the even field the image contents are displayed at a position 34 pels to the left of its last location. In this fashion the document images appear to move smoothly from right to left across the display.

For shift-left presentations in the intermittent mode, the document image moves rapidly until centered on the screen, then stops. Timing for this option can be varied. For instance, if the image should be at rest for about 0.7 second, then the motion must be completed in about 0.3 second. If the image moves 64 pels per field time, the display width (1024 pels) will be traversed in 16 field times or 0.267 second. This leaves the image at rest in the center of the display 0.733 second.

For shift-down presentations, the same procedure may be used as that used for shift-left presentations by exchanging rows for columns. This presentation produces address fields coming in from the top, stopping in the center of the display area, and disappearing from view at the bottom as a new address field image is presented.

In an alternate mode of presentation the screen would be divided into two each 8-inch by 4-inch sections, one above the other. The information regarding an address field would be restricted to an 8-inch-wide by 4-inch-high area on the display. Since these images closely approximate life size, the height of the address field on the belt would be restricted to 4 inches in the direction of envelope motion.

This restriction of size in the direction of copy motion probably can accommodate a preponderance of mail, including all envelopes of legal or smaller size. Some recognizable pattern applied to the belt could produce a recognizable code to the scanner indicating that the mail piece has a height no greater than 4 inches and that an 8- by 4-inch display area for the operator is adequate for displaying the address field.

At the operator station, the viewer would perceive an image in the upper 8- by 4-inch half of the screen for 1 second. Then a second image would be presented on the bottom of the screen for 1 second and a new image would appear at the top. The operator then must alternately view the upper and lower halves of the image area in order to encode the address information.

There may be some advantages to this mode of presentation since each document may now reside on the display for a period approaching 2 seconds, even though the encoding rate remains at one document per second. Upon finishing the classification and encoding of one envelope, the operator may immediately begin to perceive information on the alternate display or may spend a few tenths of a second more than the allotted 1 second to complete the classification of an address field with which he has difficulty. In some instances with easily legible addresses, he can recover the lost tenths of seconds on the next mail piece.

There are other forms of displays which can be tested. These include such imagery techniques as lap dissolves, in which one image fades as another is brought into distinct view. A second alternative would be the ability to fade to black between each image pair so that the operator has a distinct confirmation that his entry from the preceding image is complete and that new information is now available.

Without otherwise testing these as well as other information display formats, it is difficult to predict which might produce the highest accuracy and throughput rate over a long period. If testing cannot be accomplished before the final configuration must be implemented, it is recommended that the flash image replacement technique be used as the primary method.

Throughput timing tradeoffs. Experience with the letter sorting machines shows that given sufficiently legible address fields, a human operator can make the proper entries for Postal Service sorting schemes at a 1-second-per-document rate. But with the document characteristics to be accommodated by the MRVS, it is not certain that an operator can perceive and make decisions at a uniform 1-second interval. Some of the alternatives to this timing are as follows:

> Maintain a 1-second interval and allow the defaulted mail to be recirculated on a delay loop belt mechanism.
>
> Provide asynchronous timing for the displays.
>
> Mix the alternatives mentioned above among various work stations.

One alternative for timing of the work stations with MRVS is to establish a mean time for display and keyset entry based on the results of actual studies. The studies should be based on reviewing the performance of a multiplicity of operators by using one or more standard mixes of mail typical of predicted MRVS input, then determining the error rate, recirculation rate, and operator fatigue factors. In a properly controlled test, it should be

possible to determine which subset of MRVS-class mail causes the most difficulty, yields the highest error rate, and causes the preponderance of operator fatigue.

Once these parameters have been determined, it is possible to formulate a strategy for establishing the display timing requirements for the work stations. For instance, it may be that documents in legal and smaller envelopes may be accommodated with high throughput even though the legibility of the address field is a problem. Major problems may occur with address fields on flats, circulars, and periodicals that are larger than legal-sized envelopes. Therefore, it may be possible to mechanize the appropriate sensors at the scan head so as to differentiate and sort between legal size and smaller vs the larger mail piece configurations. The system can be programmed to assign the smaller class of mail to a majority subset of operators whose throughput timing is rigorously set at the 1-second rate, and the remaining minority of operators can be allowed to operate asynchronously in coding the address information as decisions are reached.

Unless the preceding evaluation of operator performance versus level of document difficulty is accomplished, NOSC recommends that the principal method of presentation be restricted to the standard 1-second interval with the option of keying the document into a recirculation loop, allowing a second pass by the same or another operator.

SYSTEM ALTERNATIVES

We have described in a sterile way, a proposed system which might be specified, fabricated, and installed. It is felt that guaranteeing rapid throughput would be a high- risk undertaking. Since there exist a number of unknown parameters regarding the system architecture and its effectiveness at the operator/machine interface, this section suggests primary system alternatives designed to acquire the parametric data needed to specify an EDM version of an MRVS that would have minimum embellishments and a high probability of rapid, accurate throughput, enthusiastic operator acceptance, and minimum per-unit cost.

SCAN HEAD ALTERNATIVES

Earlier sections discussed the problem of acquiring document address fields at the required scan rate. The problem was simply one of obtaining an adequate output signal from the sensor. This in turn related to the tradeoffs among available illumination, lens aperture and its relationship to depth of field, and the sensitivity of the sensor itself. The problems of increasing significantly the illumination available over a photopic visible spectrum were fairly well stated. Two alternatives to the scan head approach that may lead to an increase in electrical output from the scanning sensor device are described next.

Laser scanning. The R&D Lab of the US Postal Service at Rockville has procured a laser scanning system. This engineering prototype model employs a helium-neon laser and associated deflection system to provide a high-performance, agile optical beam that can be deflected over a relatively wide scan line. This prototype model, in conjunction with a photomultiplier and an adequate amplifier, may provide the necessary electrical signals to produce high-quality document images.

At present, the full performance capabilities of this equipment have not been characterized. One of its advantages is that it purportedly has a great depth-of-field capability. A second advantage is that even in the event that the present laser does not possess adequate power to provide the necessary photon-to-electron output from available photomultipliers, a larger and more powerful laser could be incorporated with this type of system to provide adequate illumination on the document for high photomultiplier output.

A disadvantage to this approach as it presently exists is that the illumination on the document is monochromatic, presently in the red end of the spectrum. The system could be configured with two lasers so that at least two major spectral lines within the visible range could be used for document illumination, thus reducing the dependence on red/black contrast ratios of mail pieces.

Note that one of the preliminary proposed planned tasks of the USPS/NOSC 1982 contract year SOW Agreement includes the possible characterization of this scanning system.

Time-delay and integration imaging. Another proposed method of resolving the sensor output problem is to use a time-delay and integration (TDI) imaging device. The US Postal Service has completed a second-phase contract with RCA Princeton, NJ, from which several prototype TDI imaging devices were delivered (to NOSC). Their dimensions are 748 pels in width by 96 sites in the direction of copy motion.

The process of characterizing these imaging devices is under way at NOSC. It is expected that this type of imaging device might provide 20 times the sensitivity of a line imager.

Although the device is only 748 pels in width, 7.48 inches in width can be accommodated at a scan density of 100 pels per inch on the document. A density of approximately 100 pels per inch may be adequate for this application. Conversely, if more pels are required, a continuing phase of effort between the USPS and RCA may be undertaken to produce imaging devices having scan widths of 1700 or 2200 pels. Preliminary results of the characterization of the 748-pel devices should be available around mid-1982.

IMAGE DATA STORAGE AND DISPLAY ALTERNATIVES

The section on the display and refresh control processor describes a conceptual final configuration for the display and refresh control processor. This design was conceived without benefit of experience with systems similar to the one actually required for MRVS.

It is felt, therefore, that it is in the best interest of USPS to design, acquire, install, and evaluate a great number of alternative options to the system described earlier.

PROPOSED DEVELOPMENT SYSTEM

SYSTEM CONFIGURATION

It is proposed that NOSC assemble an MRVS development system for use in developing system and operational requirements for MRVS. The equipment would initially reside at NOSC for the first phases of system requirement development. When NOSC can demonstrate several alternative system architectures, the system control software, and alternative soft-copy display formats, NOSC would ship the hardware to USPS R&D Labs at Rockville for evaluation of these alternatives. Also, the development system can then be interfaced to a prototype or development model mail transport system as it is delivered to USPS.

A block diagram of the proposed system is shown in figure D5. The CPU chosen for the system is a DEC PDP-11/34A minicomputer with a full complement of 128k words of MOS memory and the RSX-11M operating system. CPU peripherals include a VT100 CRT terminal for system control and software development, a line printer for software development and operational statistics hard-copy output, two RL02 10.4-megabyte disks for developmental software storage, and an 800/1600 BPI dual-density magnetic tape unit with controller to be used for transporting images and software to/from NOSC.

The image processor and display controller is a DeAnza IP8500 Series Image Array Processor configured with 12 image memories, two 512 by 512 video output controllers, one digital video processor, one 1024 by 1024 video output controller, DeAnza's library of image processing software (LIPS), a special high-speed interface for the CPU, and a 300-megabyte Winchester disk. The video output controllers are interchangeable, ie the IP8500 can be configured as either a 512- by 512-pel system or a 1024- by 1024-pel system. This is accomplished by exchanging card sets in the chassis.

For soft-copy display output, three Conrac QQA-15 CRT monitors are recommended. These displays are capable of presenting either 512- by 512-pel images or 1024- by 1024-pel images. The display video bandwidth is 3C MHz, which is good for 512 by 512 imagery and marginally acceptable for 1024 by 1024 images.

The equipment described thus far is all commercially available, and no special engineering effort is required. It could be purchased and assembled with only a normal purchase cycle delay. As testing is done and system requirements are developed, NOSC can specify and/or develop prototype equipment for such items as the right/left-handed keysets (if they are not already available from USPS sources), image acquisition station mockups, image buffer memory, image histogram generator and, if required, image enhancement hardware. Some of the initial tests to be performed on the demonstration system are outlined next.

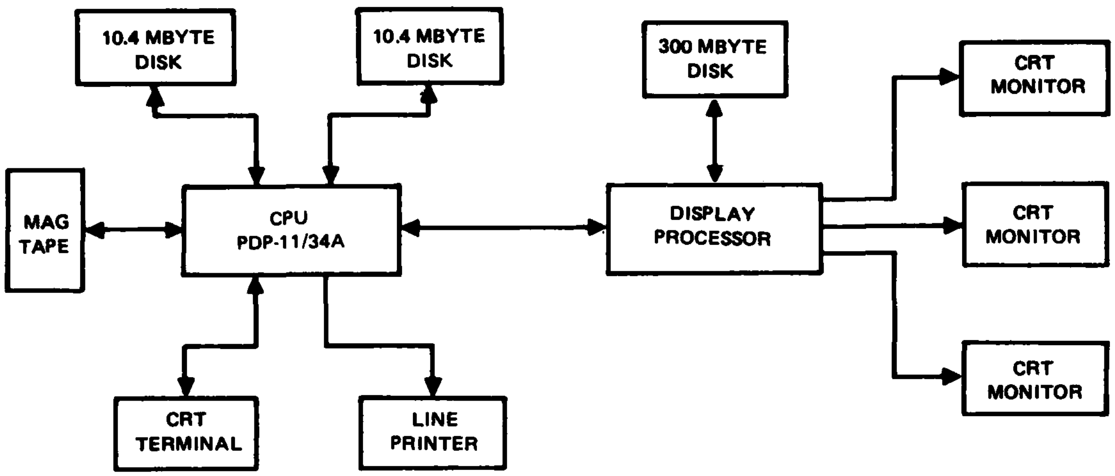


Figure D5. MRVS development center.

SOFT-COPY DISPLAY FORMATS

The requirements of the soft-copy display format dictate to a fairly large extent the complexity of the hardware required to implement MRVS. The initial guidance given to NOSC for the display format requested 1-bit (bilevel) video in a 1024 by 1024 display about 8 inches square that displays an 8-inch-square area of the mail piece. It is recommended that several alternative display formats such as the following be investigated.

1024 by 1024 display showing an 8-inch-square area of each mail piece with subsequent images scrolled downward from the top

1024 by 1024 display showing an 8-inch-square area of each mail piece with subsequent images scrolled from left to right

1024 by 1024 display showing an 8-inch-square area of each mail piece with subsequent images flashed onto the screen

1024 by 512 horizontal split-screen display showing a 4- by 8-inch area of a mail piece in each half of the display and with subsequent images flashed into the portion of the display containing the older image

512 by 512 display showing an 8-inch-square area of each mail piece with downward scrolling

512 by 512 display showing an 8-inch-square area of each mail piece with left/right scrolling

512 by 512 display showing an 8-inch-square area of each mail piece with subsequent images flashed onto the screen

Other variables to be tested include varying the scanning resolution to display smaller areas of each mail piece, eg a 4-inch-square or 6-inch-square area. Also to be tested is the grey scale resolution of the imagery, ie whether 1-bit video or 4-bit video is easier for the operators to interpret. If 1-bit video is decided upon, then a suitable means of thresholding must be found. NOSC has experience with several different approaches to thresholding.

Using ICAS, NOSC can scan representative mail pieces at various resolutions for use on the development system to demonstrate the various display formats, grey-scale resolutions, and thresholding schemes.

OPERATOR INTERACTION

Several aspects of operator interaction with the system need to be explored in more detail before the final system specification can be generated. The first of these is the selection of the desired display

format. To make this selection it is proposed that at least three work stations be assembled as part of the demonstration system so that chosen USPS personnel may evaluate system alternatives.

The actual keyset to be used by the operators has not yet been chosen. This demonstration system will allow testing of different keyset formats as well as any special function keys that may be required as a result of testing the various system alternatives. One possible function is that of controlling the scanner. If a recirculating transport system is selected, then it would be possible for an operator to key in a code that tells the scanner to scan a field shifted left, right, up, or down if the first pass missed the actual address area. If the address is orthogonal to the regular scanning direction, a mechanism must be provided to cause the image to be rotated 90 degrees the next time that mail piece is scanned.

APPENDIX E

HARDWARE ILLUMINATION CORRECTION
AND
HARDWARE EDGE ENHANCEMENT
PERFORMANCE EVALUATION

by

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Code 7323

APPENDIX E CONTENTS

APPENDIX E ILLUSTRATIONS

OBJECTIVES

The objectives of this appendix are to review the NOSC efforts on the algorithm generation for illumination correction and edge enhancement, to describe the hardware designed and built by Data/Ware Development, Inc, and to provide examples of images processed by the hardware illumination corrector (HIC) and the hardware edge enhancer (HEE). Recommendations are also derived from the analysis of the processed images. Possible alternative approaches to processing facsimile-type images for the USPS are suggested for use in equipments for future electronic mail systems.

BACKGROUND

NOSC investigations in the area of high-speed facsimile scanning under earlier USPS contracts included corrections for scanner nonlinearities and image enhancement techniques for increasing the compressibility of image data. The requirements placed on the investigation included the requirement that any algorithm developed must be able to be reduced to hardware that can process image data at real-time rates. Initial requirements included the processing of information at 20 pages per second, which, at a scanning density of 200 pels per inch, equates to 84 megapels per second. But because of limited ability to handle paper at rates much over five pages per second, the overall system requirements have been reduced to the five-page-per-second rate. This reduces the pel rate to about 20 megapels per second at a scanning density of 200 pels per inch. It is thus a reasonable task to design digital hardware to process image data at this rate.

An unsolicited proposal was received from Data/Ware Development, Inc, for two hardware units that would perform illumination correction and edge enhancement at rates up to 20 megapels per second. The proposal was based on descriptions of the algorithms published in references E1 and E2. Contract deliverables included a hardware illumination corrector, an expansion memory unit, a hardware edge enhancer, and a GNAT System 10 microcomputer. This equipment has been interfaced to the Image Capture and Analysis System (ICAS) and has been successfully operated at the 20-megapel-per-second data rate.

E1. NOSC Technical Report NELC TR 1965, First Annual Report, Advanced Mail Systems Scanner Technology, October 1975, DTIC AD A020175.

E2. NOSC Technical Report NELC TR 2020, Second Annual Report, Advanced Mail Systems Scanner Technology, vol 1, October 1976, DTIC AD A039962.

ALGORITHM DEVELOPMENT

ILLUMINATION CORRECTION

The initial analyses of early scanner data revealed a need to compensate the data for nonlinearities, which occur in most parts of the data acquisition system. Initial tests used the following equation for the illumination correction of scanner data:

$$P_{out} = \frac{CV_{max}}{CV} P_{in} ,$$

where

P_{in} = input pel

CV_{max} = maximum value that a calibration value may have

CV = calibration value for the same pel position along the scan line as P_{in}

P_{out} = the corrected pel value

Several reports have been written to describe the many tests performed relative to illumination correction, and they can be found in references E2 through E6. Earlier tests have shown subjectively that there is an improvement in the quality of corrected images when the precision of the calibration values is increased from 6 to 10 bits for 6-bit images. Annex A to this appendix presents a detailed quantization error analysis of the illumination correction procedure. The total error introduced by both the quantization of the data and the illumination correction procedure is as follows:

$$\text{Error} \quad \frac{W_{max}}{W} \quad \frac{1}{2^{N+1}} + \frac{1}{2^{M+1}} + \frac{1}{2^{N+1}} ,$$

E3. NOSC TR 170, Third Annual Report, Advanced Mail Systems Scanner Technology, October 1977, DTIC AD A051508.

E4. NOSC TR 358, Fourth Annual Report, Advanced Mail Systems Scanner Technology, October 1978, DTIC AD A070546.

E5. NOSC TR 520, Fifth Annual Report, Advanced Mail Systems Scanner Technology, October 1979, DTIC AD A089436.

E6. NOSC TR 642, Sixth Annual Report, Advanced Mail Systems Scanner Technology, October 1980, DTIC AD A097493.

where N is the number of bits in the image data and M is the number of bits in the calibration values. This means that for 6-bit (N = 6) images corrected with 6-bit (M = 6) calibration values, the magnitude of the error can approach 2-1/2 quantization levels at either edge of the image if there is a 50% droop in the system response, and 1-1/2 quantization levels at the center of the image. But when 8-bit calibration values are used on 6-bit data, the error is reduced to 1-3/4 quantization levels at the edge and 1-1/8 levels at the center of the image. It has been observed that increasing the precision of the calibration values beyond 8 bits doesn't produce any noticeable improvement in image quality. Thus the procedure has reached the limits of overall system noise, which is probably around 2% of full scale.

When 8-bit calibration values and 8-bit image data are used, the error is still 2-1/2 quantization levels. These quantization levels are for 256-level rather than 64-level data, and the resulting uncertainty is reduced from 3.9% (2.5/64) to 0.98% (2.5/256). The latter is below the 2% estimated present system noise level and is adequate for the current application.

For evaluation purposes, the HIC was designed to accommodate 6-bit or 8-bit pel data and up to 10-bit calibration values.

EDGE ENHANCEMENT

As presented in the First Annual Report (reference 1), the edge enhancement algorithm is given as follows:

S_1	S_2	S_3
S_4	C	S_5
S_6	S_7	S_8

C = center pel to be enhanced

S_i = the eight pels surrounding the center pel

Output $O = C(2K + 1) - K(S_{highest} + S_{lowest})$

K = gain constant of enhancement with a range of 0 to 1

Exception: If $C \geq$ every member of S_i, then $O = C$.

To simplify the actual implementation of this algorithm in hardware, the equation was rewritten to include a new gain constant M, where M = 2K, as

$$O = C + M(C - (S_{highest} + S_{lowest})/2).$$

This new gain constant, M, has a range of 0 to 2.

Another consideration in the implementation of this algorithm is the edge condition, ie when the center pel is at the edge of the image, whether it is along the top or bottom line or whether it is at the beginning or end of a line. There are several ways of handling the problem. Mathematically, a preferable way of performing the algorithm is to replicate the top and bottom lines and the left and right columns of the image so that when the three-by-three kernel is centered on the first pel of the first line there are valid data in the surrounding pel positions of S_1, S_2, S_3, S_4, and S_6. This will allow the enhancement algorithm to perform properly and not output invalid data. Another way some systems perform such algorithms is to ignore the edge conditions and keep track of how many pels at the edge of an image are "garbage" pels. This is considered unacceptable for possible future electronic mail systems applications since a customer will not want random borders at the edges of documents.

In the hardware design of the HEE, a compromise solution was actually implemented. Since the scanner outputs lines of image data continuously, the line immediately preceding the active image area to be captured and the line immediately following the last line to be captured are used in place of the replicated lines. On each line then, the first enhanced pel output is actually the second pel output by the scanner, the first pel being used as a surrounding pel, S_4. At the end of each line the last pel output is replicated twice and used for the last two calculations on each line. This produces an image with no "garbage" pels.

HARDWARE ILLUMINATION CORRECTOR

The HIC is shown in block diagram form in figure E1. Three main hardware components make up the HIC. There are two 14-inch rack-mount units, one of which contains all the control logic, the calibration RAM (CRAM), and one-fourth of the function RAM (FRAM). The second unit contains the remainder of the function RAM, and the third unit is the GNAT System 10 microcomputer. The GNAT performs diagnostics on the hardware, interfaces to ICAS via the IEEE General Purpose Interface Bus (GPIB), and maintains data files for the RAM data on floppy disks.

In ICAS, high-speed data are transmitted from subsystem to subsystem over twisted pair cable at emitter-coupled logic (ECL) levels rather than transistor-transistor logic (TTL) levels in order to maintain reliable transmission at 20-MHz data rates. Therefore, as shown in figure E1, level translators must be used on the high-speed data input and output ports. These are ECL-to-TTL translators on the input ports and TTL-to-ECL translators on the output ports. Details of the interface are discussed later.

In order to scan a white standard and generate a set of calibration values there must be a data path straight through the HIC for the image data to pass unaltered into the frame-store memory (FSM). This is the uppermost data path in figure E1. It is one of the inputs to a multiplexer, which is controlled by the GNAT computer.

The calibration values (one for each pel position along the scan line) are loaded into the CRAM via the GPIB and the GNAT computer. To attain the 20-MHz processing speed, the CRAM is actually split into two parts, one for odd pel positions and one for even pel positions. The capacity of each half of the CRAM is 2k (k = 1024) words by 9 bits per word. This provides the capability of performing a correction function on up to 4k pels per line.

During a correction process, the CRAM is addressed by a pel counter that is initialized at the beginning of each line by the line sync interface control signal and that is incremented by the pel clock. This counter may be preset by the GNAT for loading data into the CRAM.

The FRAM consists of up to 128k words by 8 bits (128k bytes). It is used as a look-up table for the corrected pel values. The data for the FRAM are generated by software in the Tektronix 4054, transmitted to the HIC via the GPIB and GNAT computer, loaded into the FRAM, and stored on a floppy disk in the GNAT. To achieve processing rates of 20 MHz, this memory is actually implemented in duplicate. One memory serves the even-numbered pels and one the odd-numbered pels. Thus, there are 64k bytes of memory in the HIC chassis and 192k bytes in the memory expansion chassis.

The size requirement of the FRAM is derived as follows. An assumption was made that the scanner system response will not fall off more than 50%

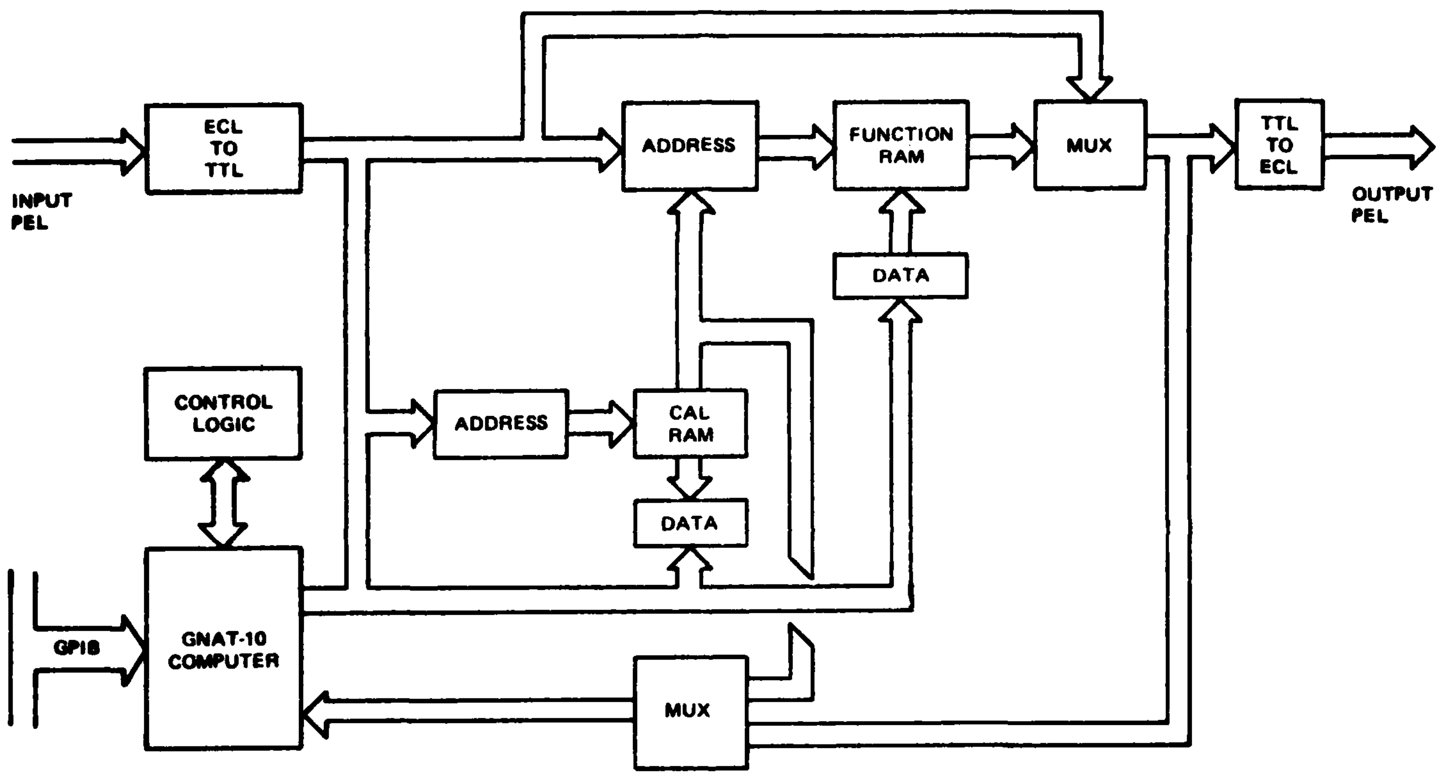


Figure E1. Hardware illumination corrector.

of the maximum response in the field of view. Therefore, the derived calibration values will always be above the 50% point, which means that the binary representation of the values will always have a "one" in the most significant bit (MSB). This allows the size of the memory to be cut to half of what it otherwise would be, ie the most significant bit of the 10-bit number does not have to be stored. The maximum size of the FRAM can thus be calculated as 2^9 times 2^8, or 2^{17}, which is 128k. This is the size of the memory required to correct 8-bit pels with 10-bit calibration values. If 6-bit pels are to be corrected, the memory size can be reduced to 32k bytes. The speed requirement then is for twice this amount of memory, ie 256k bytes or 64k bytes, respectively.

In operation, the FRAM is addressed by concatenating the 8-bit input pel value with the 9-bit calibration value for the scan line position of the current input pel to form a 17-bit address:

$$\text{Address} = P_7P_6P_5P_4P_3P_2P_1P_0C_8C_7C_6C_5C_4C_3C_2C_1C_0 \quad ,$$

where

$$\text{Input pel} = P_7P_6P_5P_4P_3P_2P_1P_0$$

and

$$\text{Calibration value} = C_8C_7C_6C_5C_4C_3C_2C_1C_0 \quad .$$

When correcting 6-bit pels, P_7 and P_6 are held at zero and thus only the lower fourth of the FRAM is addressed. It is this lower fourth of the memory that is contained in the main HIC chassis. If testing is done with calibration values of less than 10-bit precision, then the higher order bits of the 9-bit CRAM are loaded with zeros. This has the effect of skipping certain blocks of memory in the FRAM. For each of these different cases, different sets of data must be calculated for, and stored in, the FRAM.

There is a considerable amount of built-in test capability incorporated into the HIC. Data paths and control logic have been designed to allow the GNAT to write test data into both the CRAM and the FRAM and to read the data back for verification. Also, the GNAT is able to pass pel data to the HIC, generate simulated control signals and clocks, and read the corrected data back out of the HIC for verification of HIC operation. There is a set of switches and associated logic in the hardware to set up a breakpoint in the image, causing selected input and output pel values to be stored and displayed on a front panel LED display. This greatly aided the checkout of system operation.

HARDWARE EDGE ENHANCER

The functional operation of the HEE is shown in the simplified block diagram, in figure E2. As in the HIC, the data input to the HEE and the data leaving the HEE are at ECL levels, and internal to the HEE all signals are at TTL levels.

Image data input to the HEE is routed to the storage register matrix as well as to a line buffer that can store a complete line of data. The output of the first line buffer goes into the storage register matrix and to a second line buffer. In this way it is possible to pass data simultaneously from three adjacent lines of the image to the enhancement algorithm.

Inputs to the first set of comparison logic are the center pel, C, and its eight surrounding pels, S_1 through S_8. This logic is implemented in six stages of pipeline processing because it takes six pel times to determine S_H and S_L, the highest and lowest values, respectively, of the eight surrounding pels. The center pel and the control signals are also carried through this logic so that all signals are delayed by the same amount throughout the HEE.

The next function performed is that of computing the enhanced pel value. This is done in four operations, the first being an add and shift to form the quantity $(S_L + S_H)/2$. Next, this value is subtracted from C. That result is then multiplied by the gain constant M. This intermediate result, $M(C - (S_L + S_H)/2)$, is added to C to form the final result. Depending on the values, there may be underflow (a negative number) or overflow (a number higher than the allowable range of pel values). There is logic incorporated into the final adder to check for underflow and overflow. A zero is output as the enhanced pel value in the case of underflow. Either a 63 or a 255 is output in the case of overflow. The 63 and 255 are the maximum values for 6-bit and 8-bit pels, respectively.

At the same time that the enhanced pel value computation is performed, a comparison is made to see whether the value of C is higher than S_H or lower than S_L, or whether $C = S_H = S_L$. If any of these conditions is met, the output pel value is equal to the input pel value rather than the enhanced value. The output logic checks for this condition as well as the underflow/overflow condition and thereby selects the appropriate value for the output pel.

In addition to the data processing hardware discussed thus far, there is a significant amount of built-in test circuitry incorporated into the HEE. The GNAT is used to perform the testing of all the hardware components described above. Data may be loaded into the line buffer memories, and the data registers and clock pulses may be generated to clock the data through the HEE one step at a time. After each clock pulse is issued, the intermediate results can be read back into the GNAT for verification.

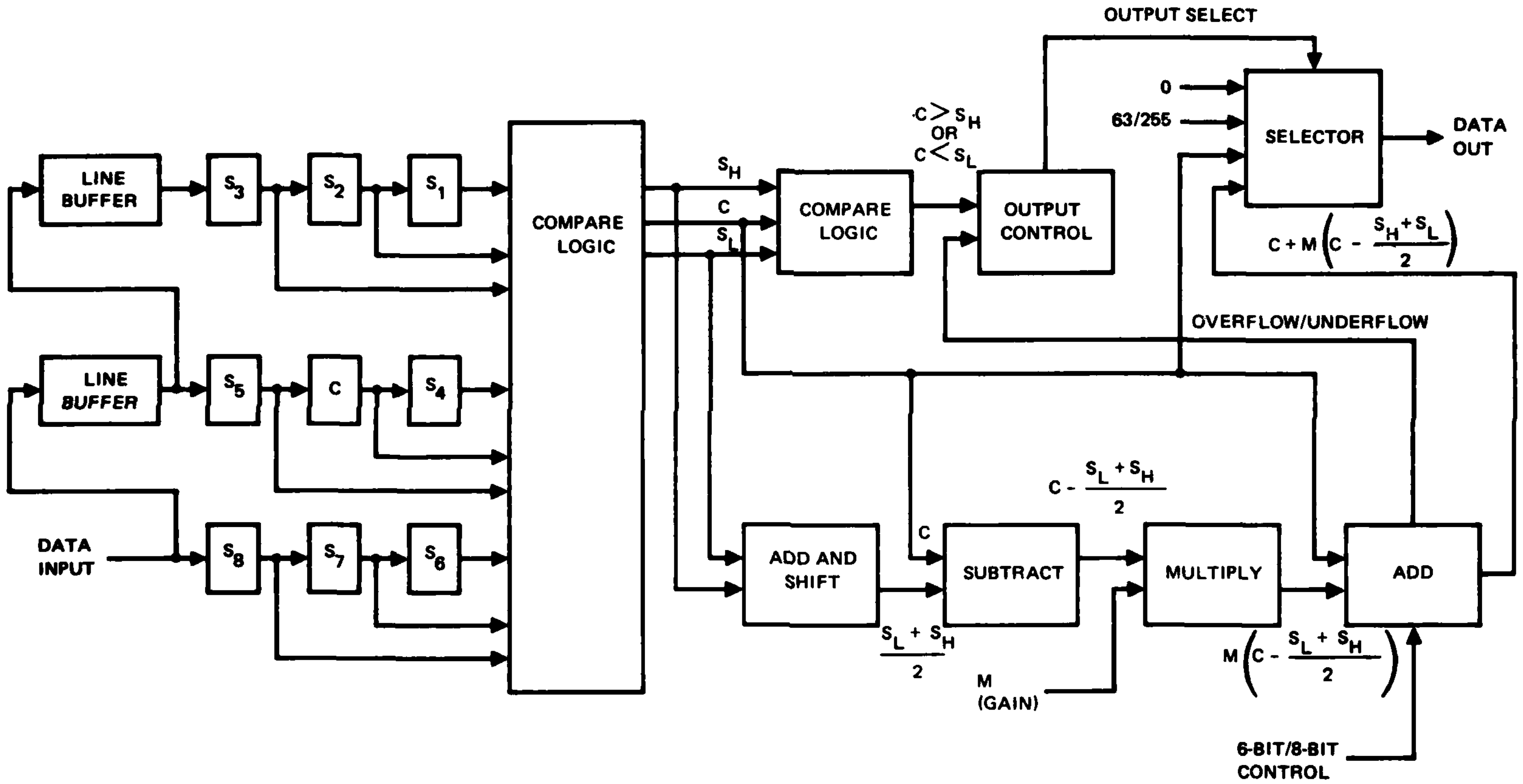


Figure E2. Hardware edge enhancer.

Front panel switches and LED displays allow the operator to monitor selected points in the computational process by using a breakpoint scheme as described for the HIC. This process requires that a repeatable data set be used. For the final debugging of the hardware, a special board was designed to store a fixed pattern of image data in a set of programmable read only memories (PROMs). This board contains eight lines of 512 pels per line and can supply the data at up to 20 megapels per second.

INTERFACE TO ICAS

Figure E3 is a system interconnect diagram showing the interconnection details of the components of the HIC and HEE system. The GNAT computer talks to the outside world via the GPIB and to the HIC and HEE via a 25-signal parallel interface. The HIC then passes the GNAT signals on to the HEE on a separate cable. The HIC and HEE decode different addresses from the parallel interface to determine which instructions to interpret and execute. High-speed image data are input to the HIC on a 13-signal twisted pair cable from the scanner. Data output from the HIC is sent to the HEE on the same type of cable with the same pinout. Data output from the HEE is sent to the personality chassis via the same type of cable. It is thus possible to route the data either through the HIC and HEE or straight to the personality chassis from the scanner. The interface between the HIC chassis and the external memory consists of three cables, two of which contain 25 twisted pairs and one of which contains 32 twisted pairs. This interface is done with ECL-level signals, as are the other high-speed data interfaces.

The system interconnection with ICAS is shown in figure E4. The high-speed data path is shown as it progresses from the scanner to the frame store memory. The data path is 8 bits wide from the scanner to the personality chassis, but it can also be logically configured to 6 bits per pel. From the personality chassis the data are demultiplexed to 48-bit words for transmission to the memory interface unit (MIU), where they are further demultiplexed to 384-bit words for storage into the Frame Store Me[illegible]

The Tektronix 4054 terminal is used for system control. I[illegible] the various units in ICAS via the GPIB, an 8-bit parallel interface [illegible] the HIC and HEE operation, the GNAT computer sends the setup parameter [illegible] data for the FRAM and CRAM to the HIC and HEE. Either the GNAT ma[illegible] commanded from its own keyboard or it can be set up to accept commands from the Tektronix 4054. The MIU contains several control registers, which are loaded from the 48-bit bidirectional data bus running between the memory control unit (MCU) and the MIU.

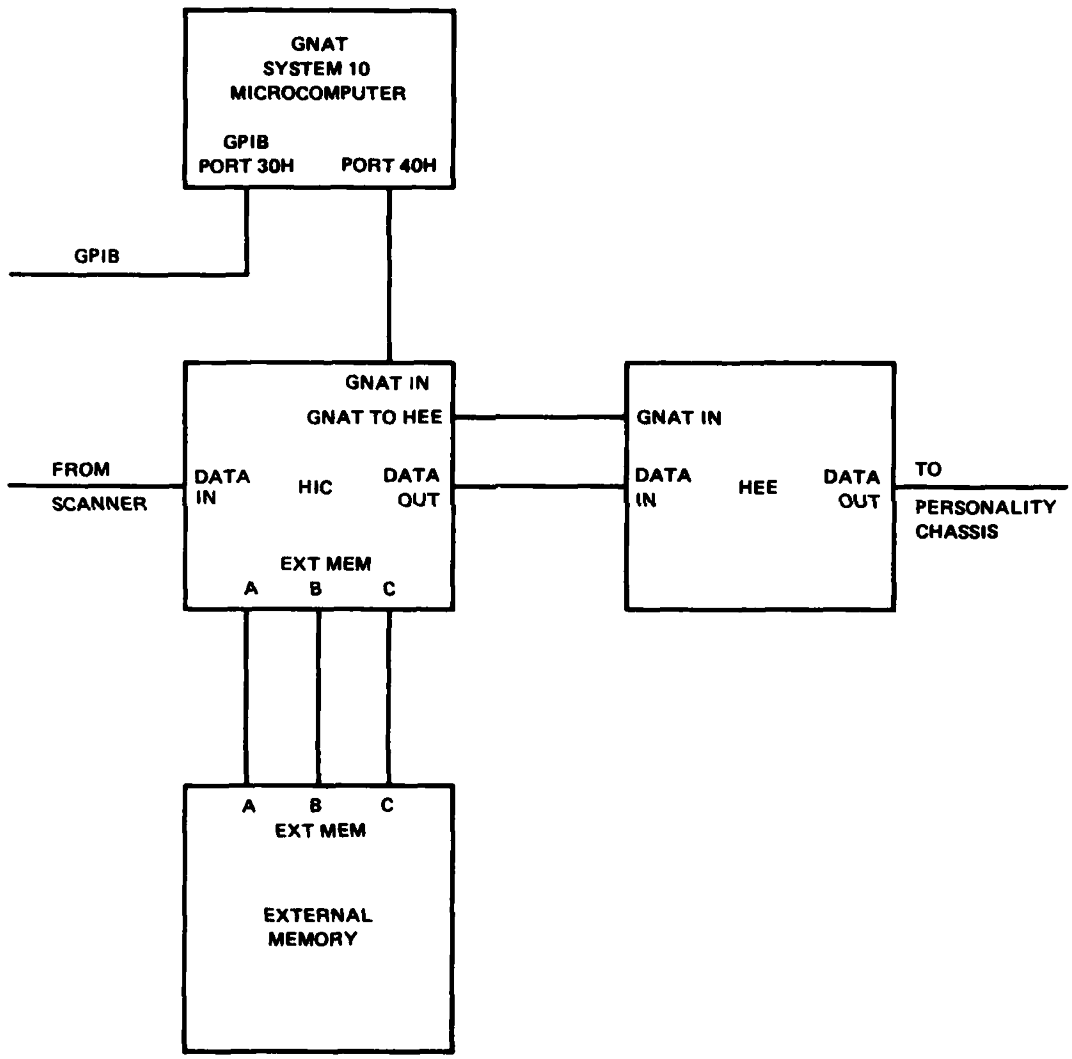


Figure E3. HIC/HEE system interconnects.

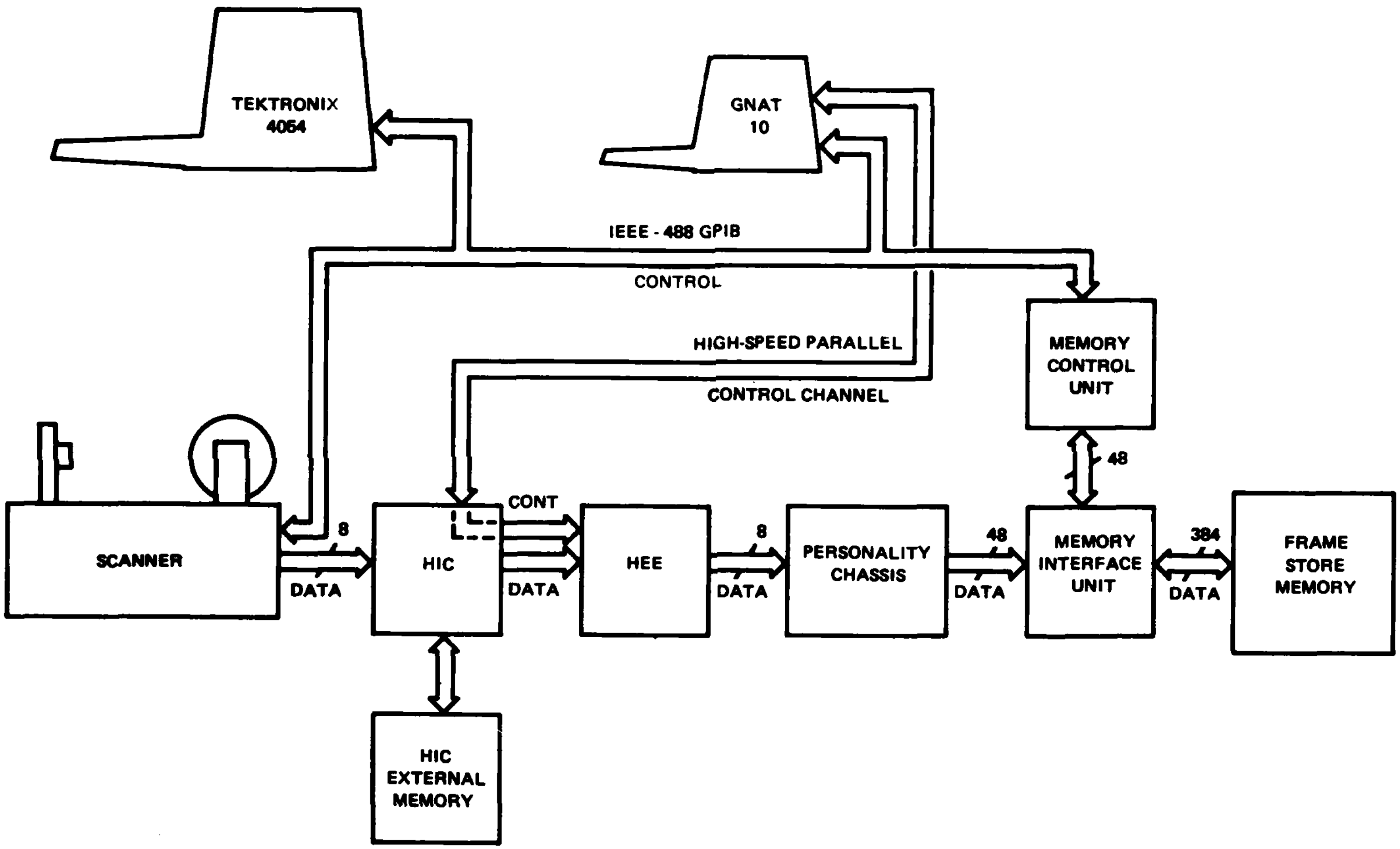


Figure E4. ICAS high-speed data acquisition path.

OPERATION

The operation of the HIC and HEE is described with the equipment set up as described in figure E4. The GNAT computer is used to control the HIC and HEE by a series of menus. The software for the system was designed for possible expansion to four complete channels. Therefore all the commands involving either the HIC or the HEE, as opposed to the entire system, require a channel number to be input as part of the command. The master menu, which appears after power-up, is shown in figure E5. The GPIB monitor mode allows the Tektronix 4054 to send command information to the GNAT. The keyboard monitor mode allows system operational commands to be entered on the GNAT keyboard and is described below. The diagnostic mode also is described later. The "examine current state" command shows what units are powered up, whether or not the RAM data have been loaded in the HIC, whether the pel size is 6 bits or 8 bits, and which units are enabled or disabled. The next five menu items are self-explanatory. The last item exits the HIC/HEE program and returns to the GNAT CP/M operating system.

```
HIC/HEE O.S. MASTER MENU
        G - GPIB MONITOR MODE
        K - KEYBOARD MONITOR MODE
        D - DIAGNOSTIC MODE
        X - EXAMINE CURRENT STATE
        A - GNAT GPIB ADDRESS CHANGE
        P6- SET PEL SIZE = 6 BITS
        P8- SET PEL SIZE = 8 BITS
        I - INITIALIZE HIC/HEE SYSTEM
        M - MASTER MENU DISPLAY
        E - EXIT BACK TO CP/M
ENTER COMMAND
!
```

Figure E5. HIC/HEE operating system master menu.

The menu for the keyboard monitor mode is shown in figure E6. If this mode is used, valid data must already be stored on the floppy disk in the GNAT for the CRAM and the FRAM. The first two options in the menu allow the data to be loaded into the CRAM and the FRAM from the floppy disk. If new data are to be generated, this must be done in the 4054 or the MCU and transferred over the GPIB to the GNAT. Options 3 and 4 enable and disable the HIC function, respectively. Option 5 allows a gain constant to be loaded into the HEE. This value ranges from 0 to 2 as described earlier but is entered as a 2-digit hexadecimal (hex) number ranging from 00 to FF. Options 6 and 7 enable and disable the HEE function, respectively. The next option shows the current status of all the units powered up, and the last option returns the program to the master menu.

```
KEYBOARD MONITOR MODE COMMAND MENU
        1# - LOAD CRAM FROM DISK (WHERE #=ID NUMBER)
        2# - LOAD FRAM FROM DISK
        3# - ENABLE HIC (CORRECTED)
        4# - DISABLE HIC
        5# - LOAD HEE "M" VALUE
        6# - ENABLE HEE (ENHANCED)
        7# - DISABLE HEE
        X - EXAMINE CURRENT STATE
        M - RETURN TO MASTER MENU
ENTER COMMAND
:
```

Figure E6. Keyboard monitor mode command menu.

The next menu is the diagnostic mode command menu, shown in figure E7. The first two options call third level menus, one for debugging the HIC and one for debugging the HEE. The third option runs an exhaustive self-test program on all units that are powered up.

```
DIAGNOSTIC MODE COMMAND MENU
        1# - DEBUG HIC MODE (WHERE #=ID NUMBER)
        2# - DEBUG HEE MODE
        3 - HIC/HEE SELF TEST
        M - RETURN TO MASTER MENU
ENTER COMMAND
:
```

Figure E7. Diagnostic mode command menu.

The HIC debug mode command menu is shown in figure E8. This menu shows that all the various data paths throughout the hardware may be verified from the GNAT to assure proper system operation. From the GNAT, input pel data may be loaded into the HIC, clock pulses may be issued, and the output data may be read back into the GNAT for verification.

The last menu is the HEE debug command menu, which is shown in figure E9. Like the HIC debug command menu, the HEE debug menu allows the operator to input data from the keyboard and clock it through the system while monitoring it as it progresses through the stages of the algorithm. Unlike the HIC, however, the HEE algorithm takes about 26 clock pulses to complete the calculation of the enhanced pel value. Also, there are 18 different registers throughout the hardware that may be monitored by using the "examine HEE registers or memory" command. This list of registers is shown in figure E10 along with the codes used for each of them. In order to utilize this

debug software effectively, the operator must know exactly how many clock pulses to issue before examining a particular register so that he may follow the progress of a single calculation through the HEE.

```
HIC (#1) DEBUG MODE COMMAND MENU
        FE - HIC FUNCTION ENABLED
        FD - HIC JUNCTION DISABLED
        P  - ISSUE PAGE SYNC
        L#  - ISSUE LINE SYNC(S)
        C#  - ISSUE PEL CLOCK(S)
        IP# - LOAD INPUT PEL VALUE
        IC# - LOAD PEL COUNTER
        IA# - LOAD FRAM ADDRESS (LSB) REG
        XC# - EXAMINE CRAM LOCATION
        XF%# - EXAMINE FRAM LOCATION (%=BLK ADDR)
        O  - READ HIC OUTPUT
        R  - RETURN TO DIAGNOSTIC MODE MASTER
ENTER COMMAND
*
```

Figure E8. HIC debug mode command menu.

```
HEE (#1) DEBUG MODE COMMAND MENU
        FE  - HEE FUNCTION ENABLED
        FD  - HEE FUNCTION DISABLED
        P   - ISSUE PAGE SYNC
        L#  - ISSUE LINE SYNC(S)
        C#  - ISSUE PEL CLOCK(S)
        IP# - INPUT PEL TO HEE
        X#  - EXAMINE HEE REGS OR MEMORY
        LM# - LOAD LINE MEMORY (2 LINES)
        R   - RETURN TO DEBUG MASTER
ENTER COMMAND
*
```

Figure E9. HEE debug mode command menu.

REGISTER CODE	REGISTER
S1	S_1 pel of matrix (line 1)
S2	S_2 pel of matrix (line 1)
S3	S_3 pel of matrix (line 1)
S4	S_4 pel of matrix (line 2)
CI	Center pel of matrix (line 2)
S5	S_5 pel of matrix (line 2)
S6	S_6 pel of matrix (line 3)
S7	S_7 pel of matrix (line 3)
S8	S_8 pel of matrix (line 3)
SH	Highest pel value of all S_i's
SL	Lowest pel value of all S_i's
Q	Q = (SH + SL)/2
K	K = C - Q
P	P = M * K
CMK	CMK = C + M * K (enhanced value)
CP	Center pel at output
M	Gain constant
O	HEE output = 0, FF, CP, or CMK

Figure E10. HEE register codes.

In normal operation of the HIC and HEE, the system is controlled from the 4054 terminal via the GPIB for almost all command and data transfers. The 4054 command menu used for this is shown in figure E11. The first operation is to scan a white standard with the HIC and HEE functions disabled, so that a set of calibration values may be generated for the current scanner configuration. This is done by averaging on the order of 1024 lines of image data from the white standard and normalizing the average to the desired maximum value and bit precision. This array of values is transferred to the GNAT and stored on its floppy disk and in the CRAM. This is done by using option 1 in figure E11. By the use of option 2, the 4054 is then commanded to generate a set of values for the FRAM, 32k values for 6-bit data and 128k values for 8-bit data. These are the computed output values for all valid combinations of calibration and input pel values. These data are also transferred to the GNAT and stored on the floppy disk and in the FRAM. If the proper data sets have already been generated for either the CRAM or the FRAM and stored on the floppy disk, then those data may be read directly into memory without being calculated again. Options 8 and 9 are used for this. This completes the required setup of the HIC, which may then be enabled to correct scanned data.

All that is required for setting up the HEE is to load the gain constant, which has a default value of 80 hex loaded during initialization, and to set the data precision to either 6 bits or 8 bits. The data precision may be set only from the GNAT keyboard. Any other desired gain may be loaded under program control. The HEE function may then be enabled to enhance data.

The HIC/HEE control functions are as follows:

1. Load CAL RAM
2. Load FUNCTION RAM
3. Activate HIC function
4. Deactivate HIC function
5. Set HEE 'M' value
6. Activate HEE function
7. Deactivate HEE function
8. Load CAL RAM from disk
9. Load FUNCTION RAM from disk
10. Generate function table
11. Utility functions

Figure E11. 4054 HIC/HEE command menu.

RESULTS

Representative samples of processed image data for a typical document are shown in figure E12. This document was scanned five times and the data were stored on tape for later analysis. To show the results easily, a small portion of each of these images was magnified by using pel replication and printed on the Dicomed film recorder as shown in figure E13. The five different modes used to scan the document were as follows:

Raw data--HIC off and HEE off
Illumination corrected only--HIC on and HEE off
Corrected and enhanced at 25%--HIC on and HEE on with gain at 40 (hex)
Corrected and enhanced at 50%--HIC on and HEE on with gain at 80
Corrected and enhanced at 75%--HIC on and HEE on with gain at CO

Not much difference can be seen between the raw data and the illumination corrected versions. But the overall effect on the images can be noticed in the pel brightness statistics for the two images, shown in figures E14 and E15. Because of the uneven illumination across the drum, the statistics in figure E14 show a rather broad peak around level 48, indicating that the background brightness varies over 10 to 12 levels. After illumination correction, the statistics show that the background level has been flattened considerably, so that 60% of the pels are contained in four brightness levels around level 48.

The lower three samples of image data in figure E13 show the results of the edge enhancement algorithm as the gain is varied from 25% to 75%. The effect of raising the background level immediately adjacent to the character edges and of lowering the level of the pels in the characters is quite pronounced. There is, however, an undesirable effect that occurs in areas of relatively constant brightness where there is a small amount of fluctuation in the intensity level. In these areas that minor variation is magnified to an extent proportional to the gain of the algorithm. This effect is discussed in appendix B, where it is recommended that the image data be spatially filtered before any enhancement is performed.

The pel brightness statistics are shown for the three enhanced images in figures E16, E17 and E18. Here, it can be seen that the overall range of brightness values is increased as the gain is increased, but that the peak value, ie the average background level, does not change in brightness. For the higher values of gain there are quite a few pels that either overflow or underflow, producing either 63 or 0 output pel values. The large numbers at the 0 and 63 brightness levels might tend to cause erroneous results when using image statistics in calculations such as those performed by the document classification algorithm. Therefore it may be advisable to disregard those two values for certain types of calculations.

One additional test that was performed on the samples shown here is that of thresholding the data. The data of figure E13 were thresholded between

ENLISTED PERSONNEL ACTION REQUEST
NAVPERS 1306/7 (REV 10-78) S/N 0106-LF-013-0636

16SEP81 | 34 | SSN [redacted]

FROM [redacted] USN, (9760/0000)

DO NOT WRITE IN THIS SPACE

TO Commander Naval Military Personnel Command (NMPC-402)

VIA (1) Commanding Officer USS JOHN F. KENNEDY (CV 67)
(2) Commander Naval Air Force U. S. Atlantic Fleet

REF (a) TRANSMAN Chapter 7

ENCL

DUTY PHONE (AUTOVON)

HOME PHONE

☐ TYPE DUTY ☐ TOUR ADJUSTMENT ☐ CHANGE OF RATE ☐ EXTENSION REENLISTMENT ☒ SCHOOL ☐ STAR ☐ SCORE ☐ SPECIAL PROGRAM

☐ OTHER Request EM "A" school (A-662-0016) on a returnable basis.
(TRANSFER EXCHANGE OF DUTY NEW CONSTRUCTION, ETC.)

DESIRED TIME FRAME	EARLIEST ASAP	LATEST
CHOICES 1ST (TYPE AREA)	2ND (TYPE/AREA)	3RD (TYPE/AREA)

REASON FOR REQUEST AMPLIFYING INFORMATION OTHER REQUEST

TO FINISH FILE (NMPC-319)
(FROM NMPC-482)

PRIOR TO TRANSFER TO DUTY REQUESTED I WILL ACQUIRE NECESSARY OBLIGATED SERVICE ☒ YES ☐ NO

IF COST TRANSFER IS NOT FEASIBLE I WILL ACCEPT TRANSFER AT NO COST TO THE GOVERNMENT ☐ YES ☒ NO

DO YOU HAVE ANY OTHER REQUESTS PENDING ACTION IN BUPERS E.G. FLEET RESERVE HUMS SCHOOLS ETC
☐ YES ☒ NO IF YES EXPLAIN ON THE REVERSE SIDE

HAVE YOU PREVIOUSLY SUBMITTED THIS REQUEST ☐ YES ☒ NO IF YES EXPLAIN ON REVERSE SIDE

PRIVACY ACT STATEMENT The authority to request this information is contained in 5 USC 301 Departmental Regulations. The principal purpose of the information is to enable you to make known your desires for the various types of duty listed, or some other special assignment consideration. The information will be used to assist officials and employees of the Dept. of the Navy in determining your future duty assignment. Completion of the form is mandatory except for duty and home phone numbers. Failure to provide required information may result in delay in response to or disapproval of your request.

Signature [redacted]

NO. OF DEPNS	LOCATION OF DEPNS	LOCATION OF HHG	EDUCATION	CITZ	CLEARANCE BASIS	FLAT
0	N/A	N/A	11YRS HS	US	N/A	N/A

If last two evaluations were E4 or below enter marks

DATE	PROF PERFORMANCE	MIL BEHAVIOR	LDRSHIP & SUPV	MIL APPEARANCE	ADAPTABILITY
31JAN81	3.2	3.2	N.O.	3.4	3.2

FROM Commanding Officer USS JOHN F. KENNEDY (CV 67) DATE
TO Commander Naval Military Personnel Command (NMPC-402)
PERS OFFICE PHONE
VIA Commander Naval Air Force U. S. Atlantic Fleet

☒ YES ☐ NO ELIGIBLE FOR DUTY REQUESTED
☒ YES ☐ NO RELIEF REQUIRED 1 MONTHS GAP ACCEPTABLE
☐ YES ☐ NO MEETS SECURITY CLEARANCE REQUIREMENTS ☒ N/A
NA YES ☐ NO SECNAV FINE REQUIRED
☒ YES ☐ NO HAS CLEAR RECORD NJP FOR PAST 7 MONTHS AS REQUIRED
☒ YES ☐ NO RECOMMENDED

SEE REVERSE FOR COMMENTS CONTINUED

MEMBERS OF SIGNATURE OF COMMANDING OFFICER
L-01262 L. W. NORDSTROM, CDR, USN, BY DIRECTION OF THE CO

NAVY TEST 1

Figure E12. Sample document N1, corrected and enhanced at 50% gain.

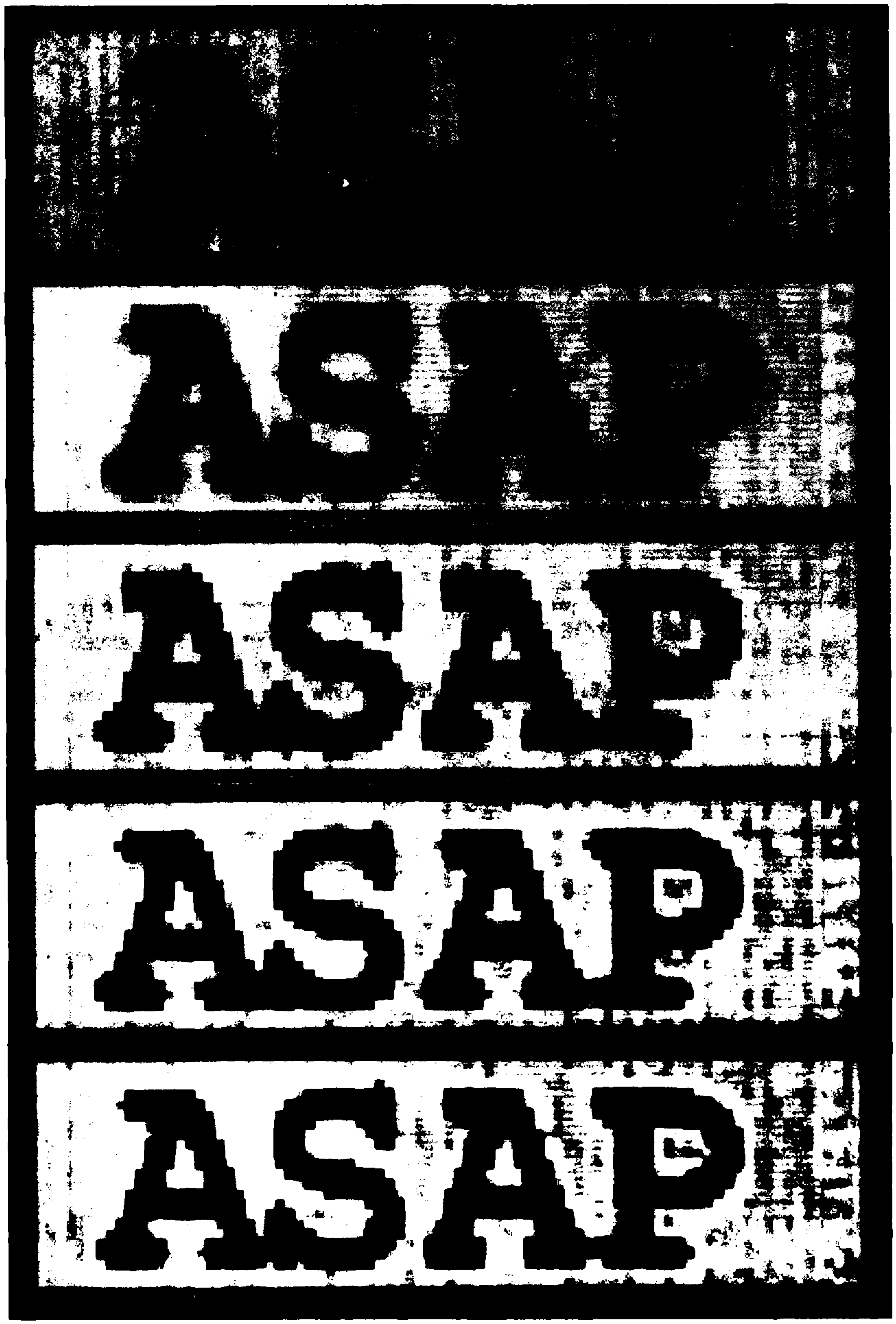
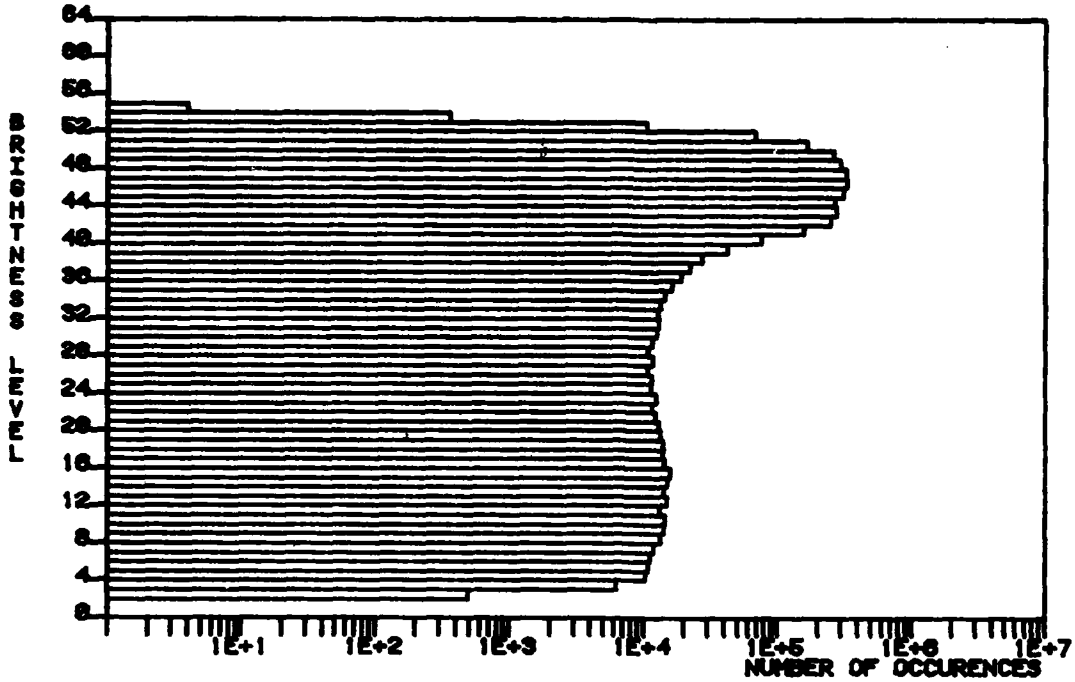


Figure E13. Enlarged samples of processed image.



Figre E14. Pel brightness statistics for raw image.

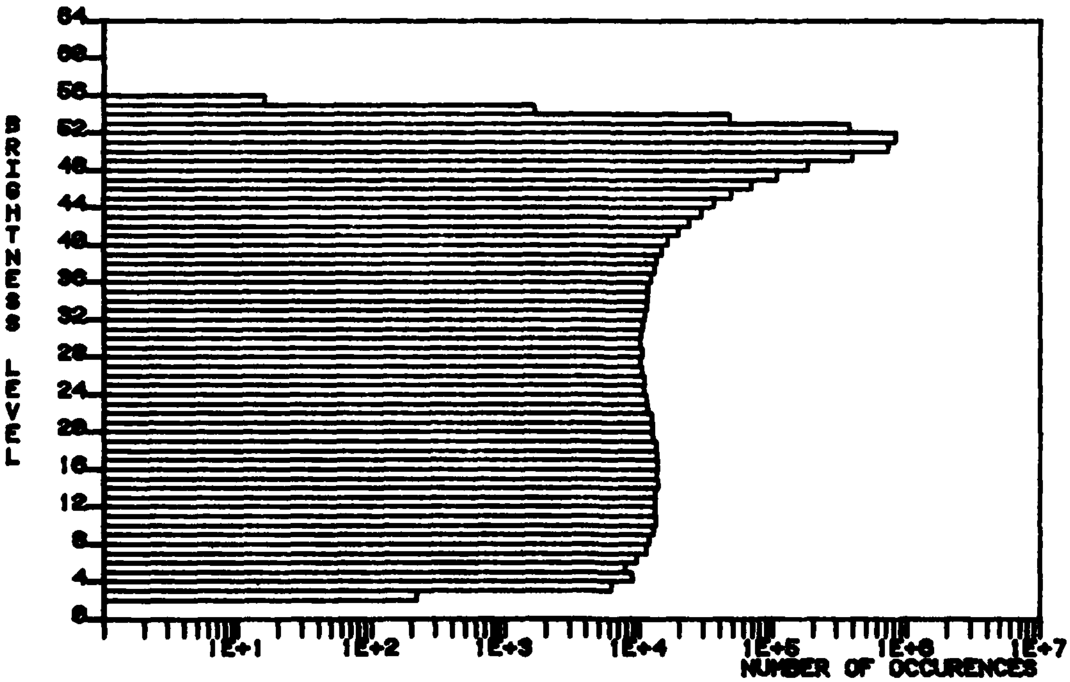


Figure E15. Pel brightness statistics for corrected image.

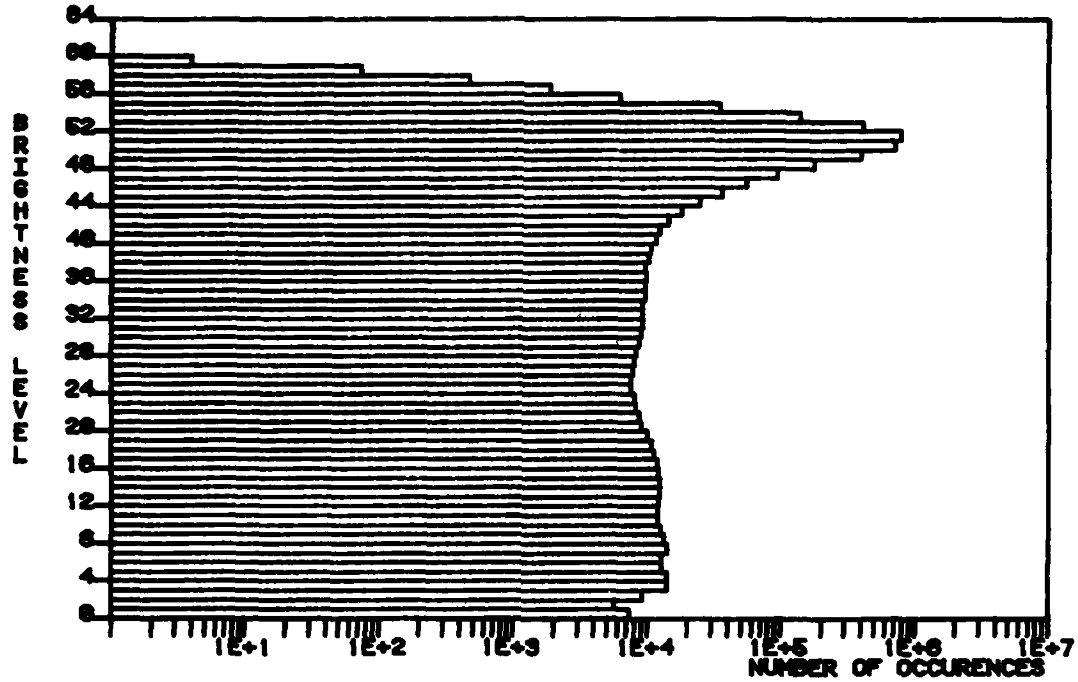


Figure E16. Pel brightness statistics for image corrected and enhanced at 25% gain.

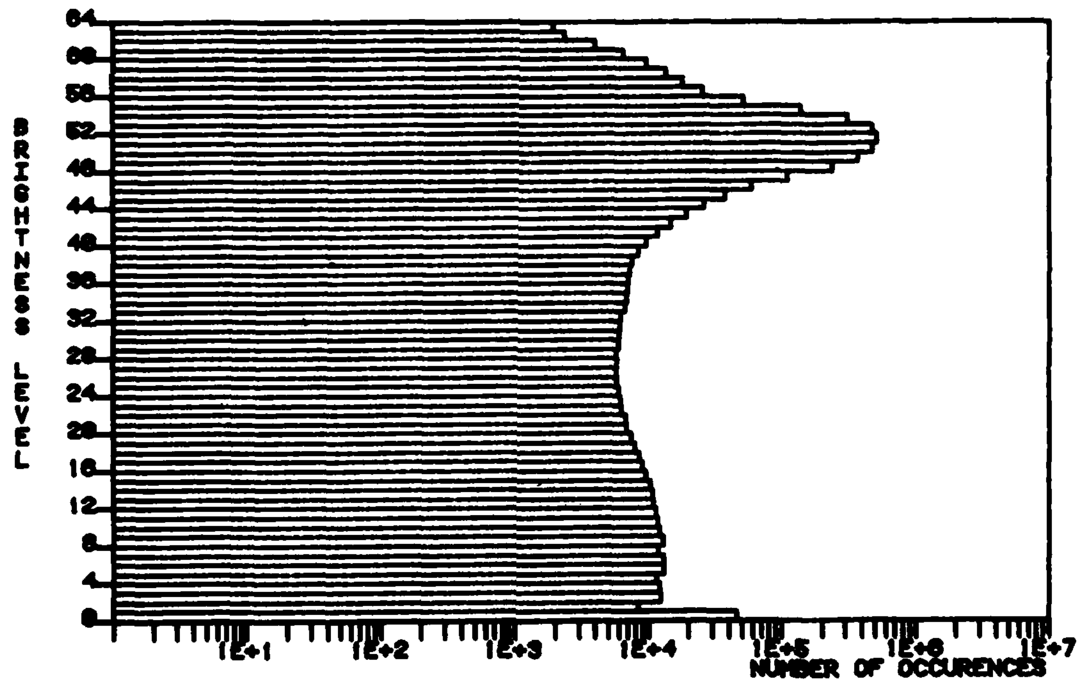


Figure E17. Pel brightness statistics for image corrected and enhanced at 50% gain.

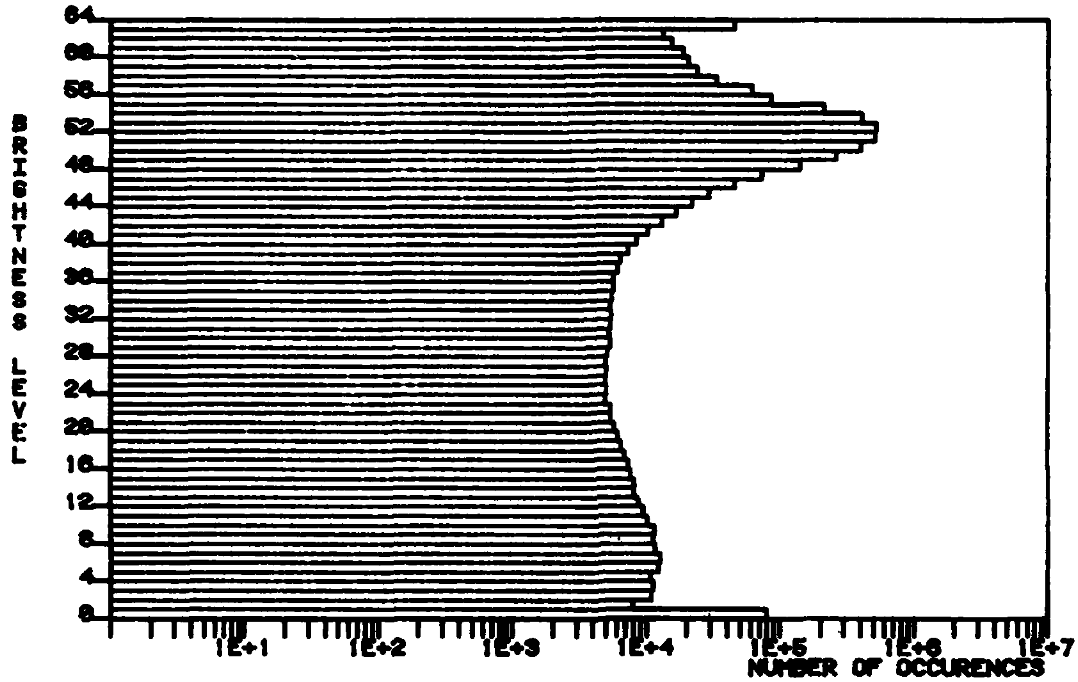


Figure E18. Pel brightness statistics for image corrected and enhanced at 75% gain.

levels 18 and 19, and the result is presented in figure E19. This threshold was arbitrarily chosen to produce the best subjective image of the typed letters. Analysis of these images indicates that there is not a significant difference between them except that the bottom image might possibly have fewer voids in the letters than the rest. All of these images would benefit from some type of filtering algorithm such as those being developed by Delta Information Systems, Inc. Representative examples are the isolated pel, the single pel on edge, and the double pel on edge removal algorithms. Details of these algorithms may be found in the interim monthly reports from Delta Information Systems, Inc, under NOSC contract N66001-81-C-454.

A representative portion of the example image was analyzed to obtain compressibility statistics for the five processed images. The results indicated that there was not a significant difference in the overall compressibility statistics for any one of the processed images. This is an indication that the correction and enhancement algorithms at least do not cause a significant increase in the numbers of runs in the various bit planes.

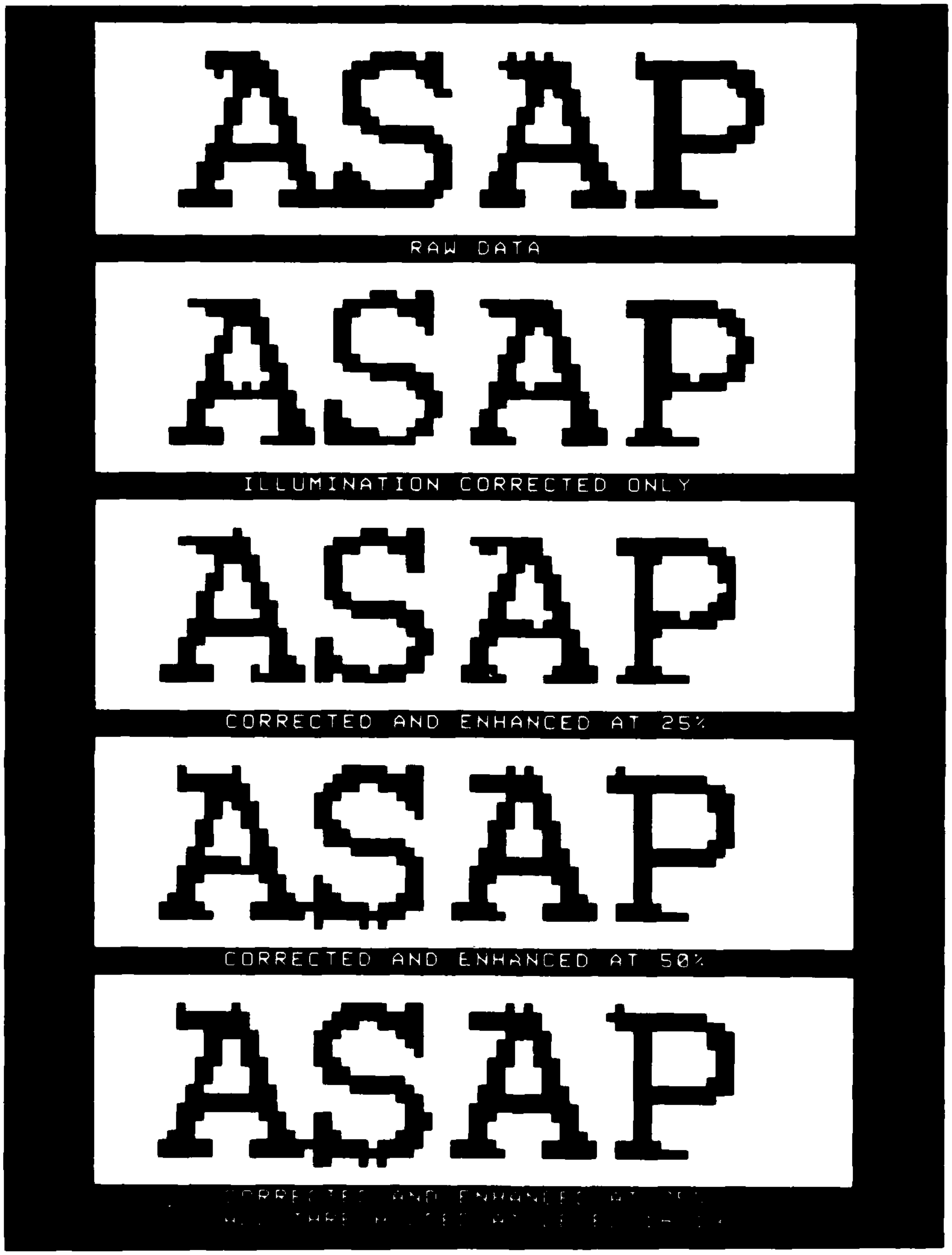


Figure E19. Thresholded version of figure E13.

CONCLUSIONS AND RECOMMENDATIONS FOR APPENDIX E

The HIC and HEE have been interfaced to the NOSC ICAS and are operational with a single-channel data stream of either 6 bits per pel or 8 bits per pel at data rates up to 20 megapels per second. Enlarged samples of typical image data were shown before and after various processing steps, indicating the effectiveness of the algorithms implemented in hardware.

The edge enhancement algorithm tends to amplify any minor fluctuations occurring in areas of an image with relatively constant brightness. Previous tests of a selective filter algorithm, described in appendix B, indicate that an improvement of about 30% is possible in the compressibility of a grey scale image by using run-length encoding. It is recommended that further tests be performed on image data with various selective filter or digital filter algorithms in software, with consideration given to implementing some form of filtering in hardware for evaluation. The reason for hardware implementation is that the logical place for the filter is after illumination correction and before edge enhancement. The current configuration of the ICAS hardware does not provide a data path from the FSM to the HEE and back to the FSM. Therefore, in order to insert a filtering operation between illumination correction and edge enhancement, both the filter and the enhancement would have to be performed in software, a very time-consuming task.

Evaluation of the thresholded image segments included herein indicates that there are imperfections in the typewritten characters in the form of bumps and voids on the character edges. Various algorithms are under investigation by Delta Information Systems, Inc, to remove single-pel and double-pel bumps on the character edges as a way of improving the compressibility of the bilevel images. It is recommended that NOSC implement those algorithms in software for testing and possible further refinement to include repair of voids in the character edges. It is also recommended that NOSC establish a communication link from the ICAS to the NOSC signal processing lab DEC PDP-11/70 computer system for the purpose of implementing the algorithms in FORTRAN, since the listings received from Delta Information Systems, Inc are already coded in FORTRAN.

REFERENCES FOR APPENDIX E

E1. NOSC Technical Report NELC TR 1965, First Annual Report, Advanced Mail Systems Scanner Technology, October 1975, DTIC AD A020175.

E2. NOSC Technical Report NELC TR 2020, Second Annual Report, Advanced Mail Systems Scanner Technology, vol. 1, October 1976, DTIC AD A039962.

E3. NOSC TR 170, Third Annual Report, Advanced Mail Systems Scanner Technology, October 1977, DTIC AD A051508.

E4. NOSC TR 358, Fourth Annual Report, Advanced Mail Systems Scanner Technology, October 1978, DTIC AD A070546.

E5. NOSC TR 520, Fifth Annual Report, Advanced Mail Systems Scanner Technology, October 1979, DTIC AD A089436.

E6. NOSC TR 642, Sixth Annual Report, Advanced Mail Systems Scanner Technology, October 1980, DTIC AD A097493.

ANNEX A TO APPENDIX E

ILLUMINATION CORRECTION QUANTIZATION ERROR ANALYSIS

This annex describes the quantization error bounds on the illumination correction algorithm developed at NOSC and used on ICAS and in the newly developed hardware illumination corrector (HIC). The error analysis is treated in terms of the digitization precision and the precision of the calibration values used for the correction process.

Figure EA1 shows a typical illumination profile generated by tabulating the data of an acquired "white standard." In this type of profile, several definitions and assumptions are made, as follows:

1. Pin_i is the input pel value at the i^{th} position along the scan line, quantized to N bits. Pin_i thus has an absolute quantization error of $e_1 \leqslant 1/(2^{N+1})$.

2. W_i is the average intensity of the white standard at the i^{th} position along the scan line. It is known to a precision of M bits, where $M \geqslant N$. That is, W_i is known to greater precision (M bits) than Pin_i (N bits) even though the values used to generate the average W_i are quantized to only N bits. This assumption can be shown to be valid if enough samples are taken for the average in the presence of Gaussian system noise. Quantization error is a uniformly distributed random variable over ±1/2 a least significant bit (LSB). Its variance is proportional to the reciprocal of the number of samples averaged and can be made arbitrarily small. The absolute quantization error of W_i is $e_2 < 1/(2^{M+1})$. Also, it is assumed that $W_i > 1$ and $Pin_i < W_i$.

3. C_m and W_m are arbitrarily defined quantities. There is no quantization error associated with them. C_m is the maximum value that the calibration values can have. It is computed as $C_m = 2^{(M-N)} (2^N - 1)$. For example, with N = 6 (6-bit pels) and M = 10 (10-bit calibration values), C_m = 1008. W_m is the maximum value of a calibration curve before the curve is normalized to C_m.

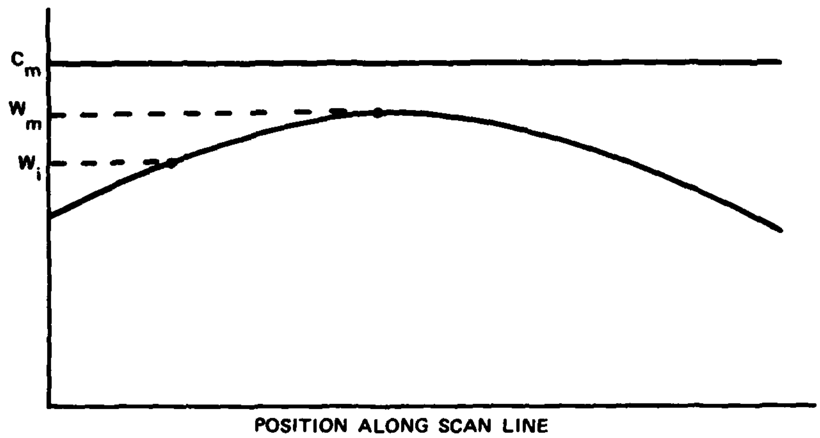


Figure EA1. Calibration Curve.

4. The procedure used in generating the calibration values is to scan a "white standard" and average some number of lines on a pel-by-pel basis; ie,

$$W_i = \sum_{j=1}^{S} P_{j,i} \quad ,$$

where S may be on the order of 1024. These numbers are then normalized to C_m, with

$$CV_i = W_i \, (C_m/W_m) \quad , \qquad (1)$$

where CV is the actual calibration value used in the correction process.

The illumination correction procedure then computes the corrected pel values according to the equation

$$\mathrm{Pout}_i = \frac{\mathrm{Pin}_i C_m}{CV_i} \quad . \qquad (2)$$

Substituting equation 1 into equation 2 and including the quantization error terms, equation 2 then becomes

$$\mathrm{Pout}_i = \frac{(\mathrm{Pin}_i \pm e_1)\ C_m}{(W_i \pm e_2)\ C_m/W_m} \quad . \qquad (3)$$

In equation 3, the subscript i implies that the associated terms are for a given pel position along the scan line. For simplicity, the subscripts will be dropped from here on, with the position sensitivity along the scan line understood. Equation 3 may be rewritten as

$$P_{out} = \frac{W_m}{W} \frac{(P_{in} \pm e_1)}{(1 \pm e_2/W)} \quad . \qquad (4)$$

The factor W_m/W is the gain associated with the illumination correction process. $(P_{in} \pm e_1)$ is the input to the correction process, and the factor $1/(1 \pm e_2/W)$ is the additional error introduced by illumination correction.

Since $e_2 \leqslant 1/(2^{M+1})$ and $W \geqslant 1$, then $e_2/W \leqslant 1/(2^{M+1})$. Also $e_2/W \ll 1$, if M is greater than about 5. The term $1/(1 \pm e_2/W)$ can then be expanded in a Taylor series as

$$\frac{1}{(1 \pm e_2/W)} \approx 1 \mp e_2/W + (e_2/W)^2 \mp (e_2/W)^3 \quad ,$$

with the second and higher-order terms approaching zero.

Equation 4 can now be written

$$P_{out} \approx \frac{W_m}{W} (P_{in} \pm e_1)\ (1 \pm e_2/W) \quad .$$

Expanding terms, this becomes

$$P_{out} \approx \frac{W_m}{W} P_{in} \pm \frac{W_m}{W} e_1 \pm \frac{W_m}{W} \frac{e_2}{W} P_{in} \pm \frac{W_m}{W^2} e_1\, e_2 \quad .$$

This may be rewritten as

$$P_{out} \approx \frac{W_m}{W} P_{in} + E_1 + E_2 \quad , \tag{5}$$

where

$$E_1 = \pm \frac{W_m}{W} e_1$$

(the scaled error of the quantized input pel),

$$E_2 = \pm \frac{W_m}{W} \frac{P_{in}}{W} e_2$$

(the additional scaled error introduced in the correction process), and the second-order term

$$\pm \frac{W_m}{W^2} e_1\, e_2$$

is dropped.

The bounds on the magnitudes of the error terms E_1 and E_2 now may be evaluated:

$$\left|E_1\right| < \frac{W_m}{W} \frac{1}{2^{N+I}} \quad , \tag{6}$$

since

$$e_1 \leq \frac{1}{2^{N+I}} \quad ;$$

and

$$\left|E_2\right| < \frac{W_m}{W} \frac{1}{2^{M+I}} \quad , \tag{7}$$

since

$$e_2 \leq \frac{1}{2^{M+I}} \quad \text{and} \quad P_{in} \leq W \quad .$$

Thus the absolute value of the error resulting from the quantization of the inputs to the illumination correction process is as follows:

$$\left|E\right| < \frac{W_m}{W} \left(\frac{1}{2^{N+I}} + \frac{1}{2^{M+I}} \right) \quad . \tag{8}$$

Up to this point, the term P_{out} in equation 5 is treated as an analog number with infinite precision in representation. This is not the case, since P_{out} must be represented as an N-bit number, as must P_{in}. Therefore, a third error term must be introduced with the same magnitude as e_1. This term represents a new quantization error, the result of expressing the output of the correction process as an N-bit number. The magnitude of the total

worst-case error will then be

$$\left|E_{TOTAL}\right| \leq \frac{W_m}{W}\left(\frac{1}{2^{N+1}} + \frac{1}{2^{M+1}}\right) + \frac{1}{2^{N+1}} \quad .$$

For instance if $N = 6$, $M = 8$ and (W_m/W) is 2 (worst case) for a particular pel position, then

$$\left|E_{TOTAL}\right| \leq \frac{1}{64} + \frac{1}{256} + \frac{1}{128} \quad .$$

This means that the uncertainty of a pel value has been increased from ±1/2 LSB before correction to ±1-1/4 LSB after correction with an 8-bit calibration value. Another ±1/2 LSB due to quantizing the final output to 6 bits is then added, yielding a total uncertainty of ±1-3/4 LSB in the resultant corrected pel value.